Innovation by Collaboration: Open Hardware Development

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The Linux Foundation: More than Linux

- **1500+** Members From 40+ Countries
- **100%** of Fortune 100 Tech & Telecom
- **30000+** Developers Contributing Code
- **200+** Open Source Projects
- **$16B+** Shared Value

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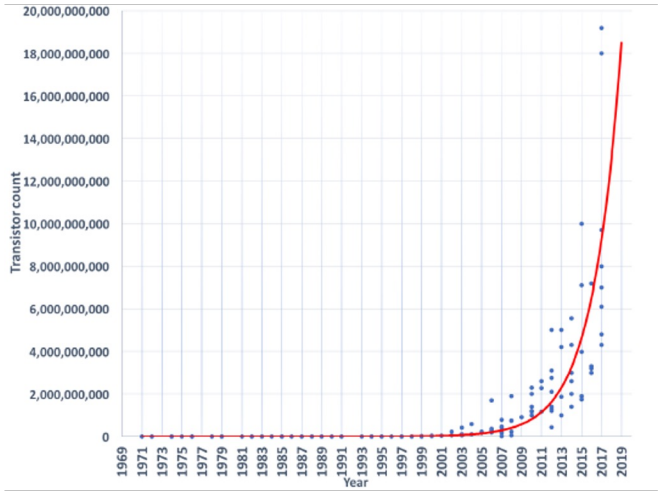
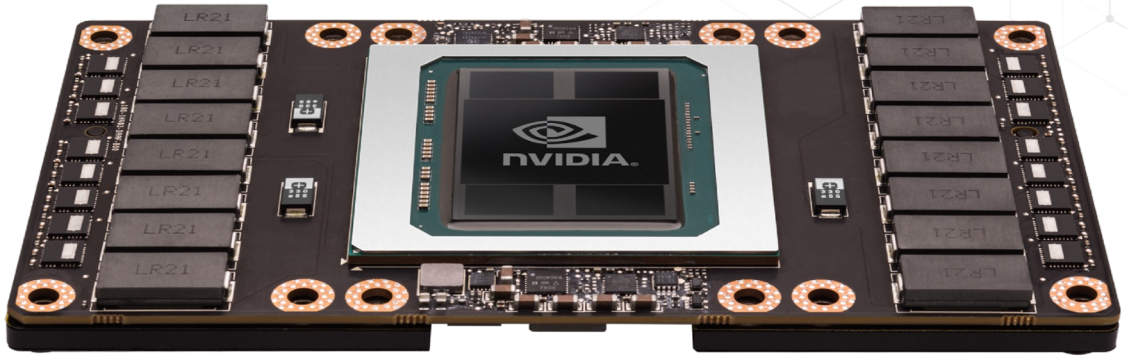
Security	Let's Encrypt, CORE INFRASTRUCTURE INITIATIVE
Networking	LF NETWORKING, ONAP, OPEN DAYLIGHT
Cloud	kubernetes, CLOUD FOUNDRY, CLOUD NATIVE COMPUTING FOUNDATION
Automotive	AUTOMOTIVE GRADE LINUX
Blockchain	HYPERLEDGER
Edge/IoT	LF EDGE, yocto PROJECT, Zephyr™
Web	node.js, JS Foundation, GraphQL
AI	LF AI
Motion Pictures	ASWF /* ACADEMY SOFTWARE FOUNDATION

Accelerating with More than Moore…

Traditional Scaling



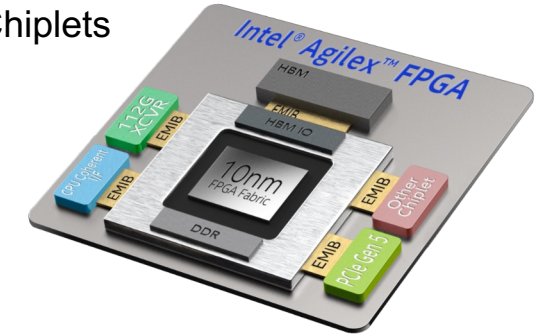
Domain Specific Architectures (DSA) : DAX, GPU, AI, FPGA



Packaging

MCM

Chiplets



Software: Compilers and Libraries

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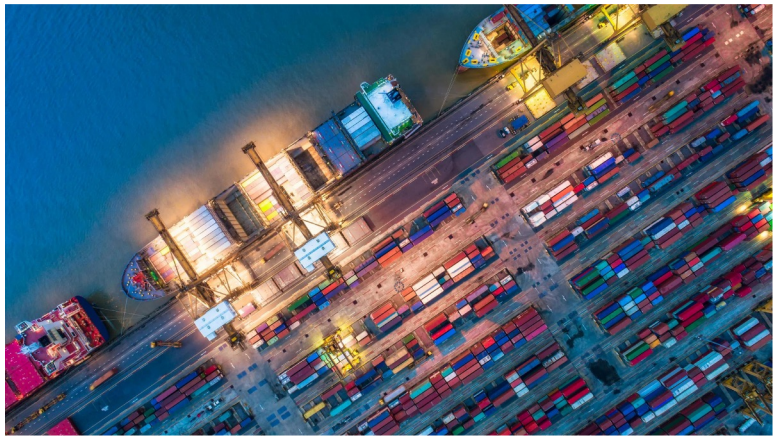
Industrial Evolution: Siloed to Collaboration

Soup to Nuts Silo: In House



Supply Chain Management: Overseer

Open Collaboration

Linux Foundation Open Hardware Development: A Neutral Territory

OpenPOWER™

RISC-V

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OpenPOWER Foundation

2013
Launched

200+
Global Corporate Members

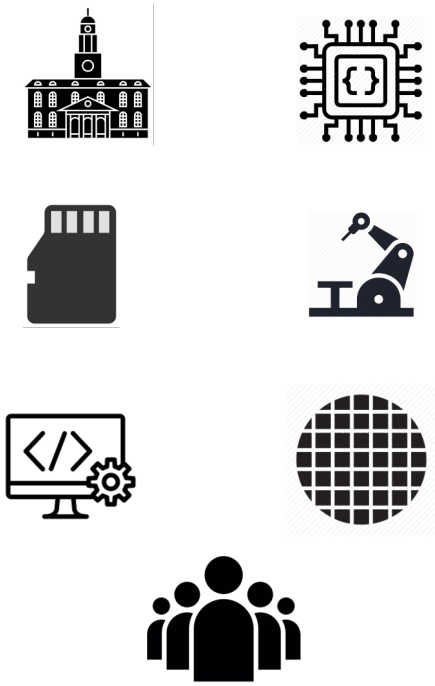
OpenPOWER Foundation is a non-for-profit organization serving its member companies and the open hardware and software POWER ecosystem

Fully open sourced POWER ISA in 2019
Moved under the Linux Foundation

OpenPOWER™

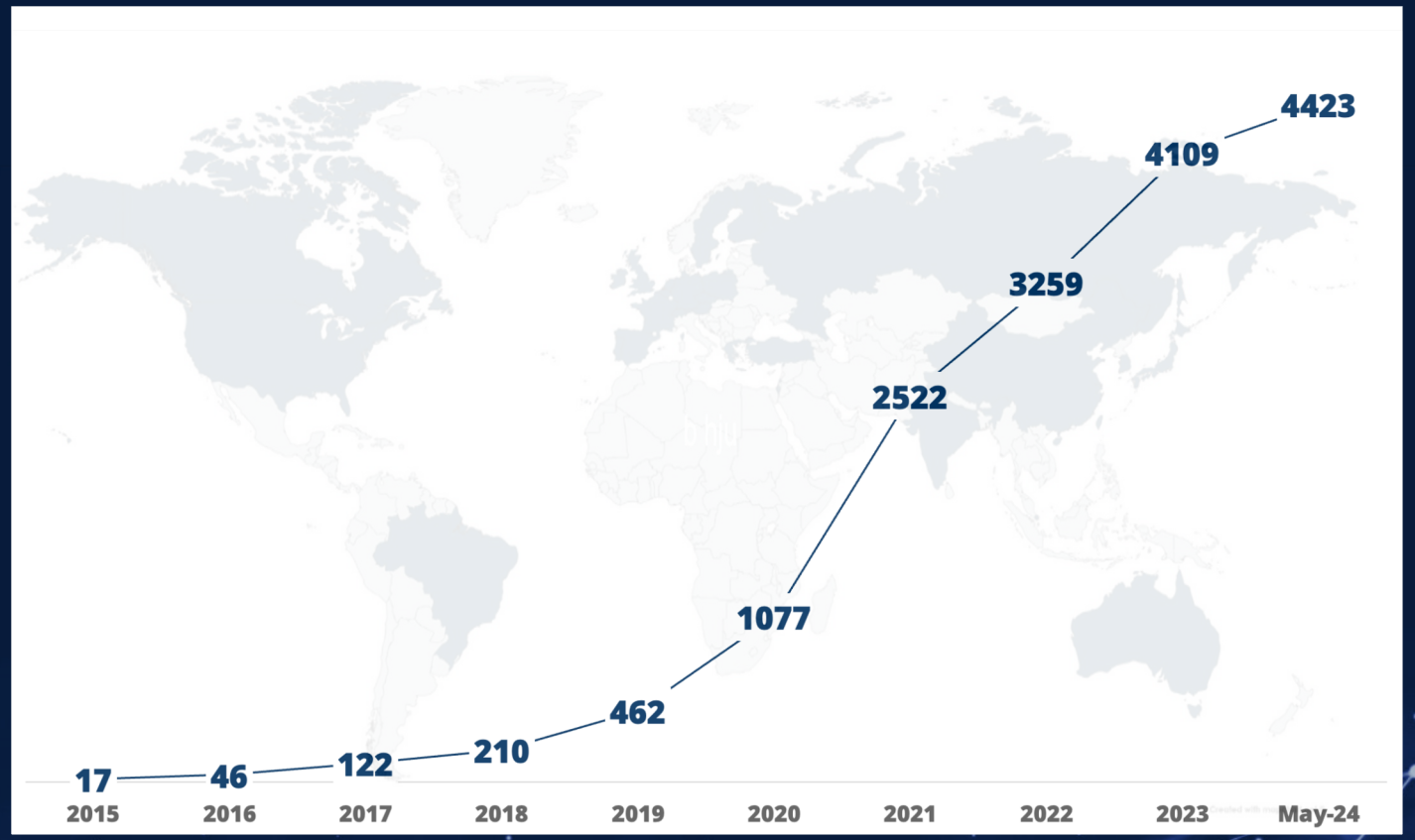
Mission: To accelerate adoption of OpenPOWER technologies including the ISA, silicon, systems, and software.

- To drive technology innovation through specifications, compliance tests, and product/technology SIGs
- To grow overall ecosystem and members
- To facilitate community engagement and collaboration, sharing of expertise and increase visibility



https://openpowerfoundation.org

More than 4k RISC-V members across 70 Countries



May 2024 update

107 Chip
SoC, IP, FPGA

4 Systems
ODM, OEM

3 I/O
Memory, network, storage

18 Industry
Cloud, mobile, HPC, ML, automotive

21 Services
Fab, design services

172 Research
Universities, Labs, other alliances

50 Software
Dev tools, firmware, OS

>4000 Individuals
RISC-V engineers and advocates

RISC-V membership up 28% in 2023

RISC-V®

CHIPS Members

Platinum Members

AMD
antmicro
FUTUREWEI Technologies
Google
Infineon
intel
Microsoft
SiFive
VeriSilicon

Auditor Members

AXIADO
Precision Innovations

Gold Members

ISCAS 中国科学院软件研究所 Institute of Software Chinese Academy of Sciences
MARVELL

Associate Members

Berkeley
BYU
ihp
RIOS
NEBRIJA
OpenROAD
RISC-V
Stanford ENGINEERING
DTU
UC San Diego
UC SANTA CRUZ
MERL
UNIVERSITY of HAWAI'I SYSTEM
MANCHESTER 1824 The University of Manchester
UNIVERSITY OF MICHIGAN
UNIVERSITY OF MINNESOTA Driven to Discover
UNB UNIVERSITY OF NEW BRUNSWICK
UNIVERSITY OF TORONTO
Yale University

Silver Members

ami
efabless
ETRI
Meta
NVIDIA
Western Digital

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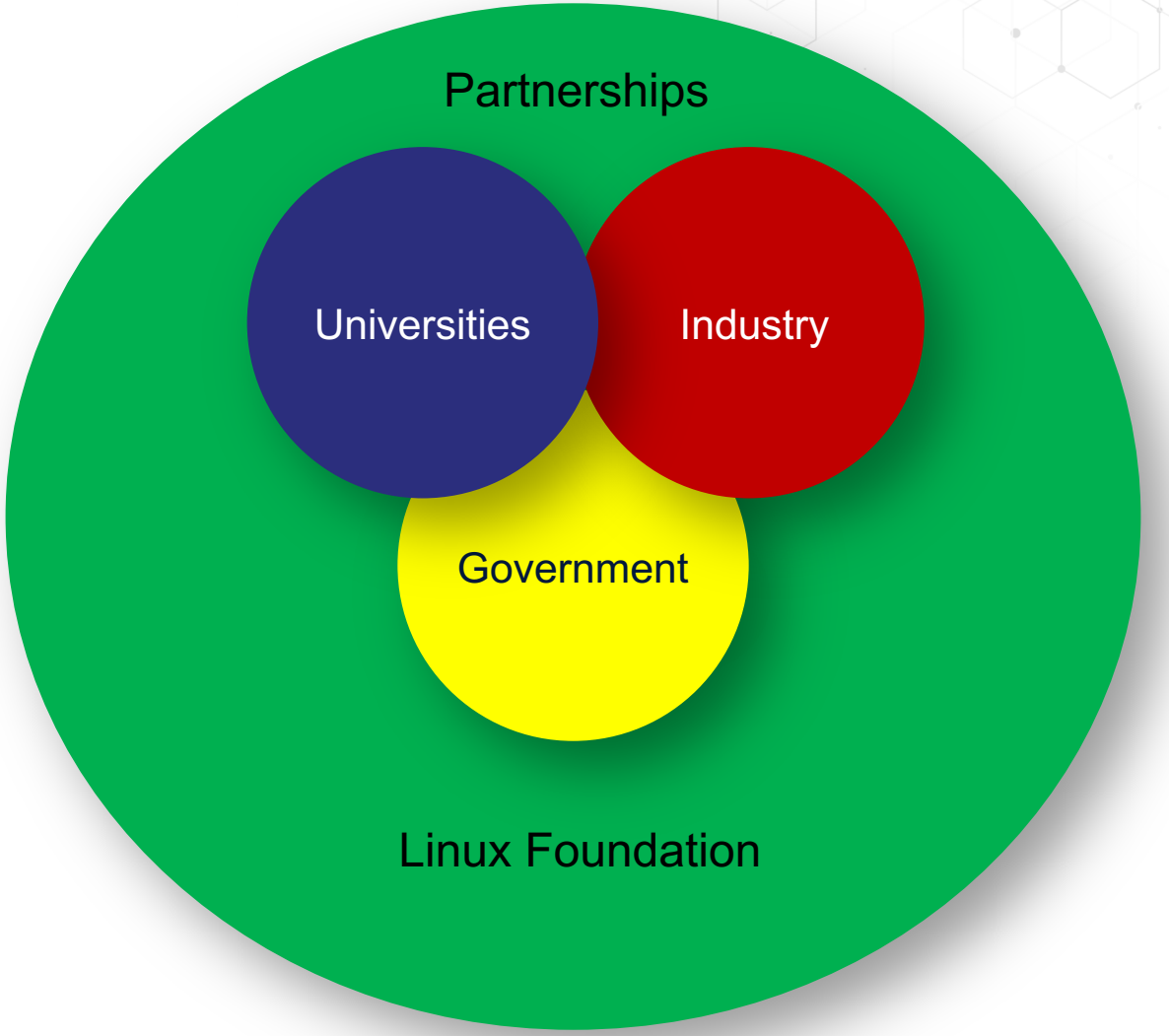
What does it take to make collaboration work?
It's not easy

- Shared common technical challenge
- Realization stronger together than apart
  - Leverage strengths
  - Willingness to share IP to move project forward
- Shared objectives
- A degree of trust
- Alignment of business, legal, engineering
- The above enables successful collaboration
- Linux Foundation is a safe harbor for collaborators to gather to solve challenging problems



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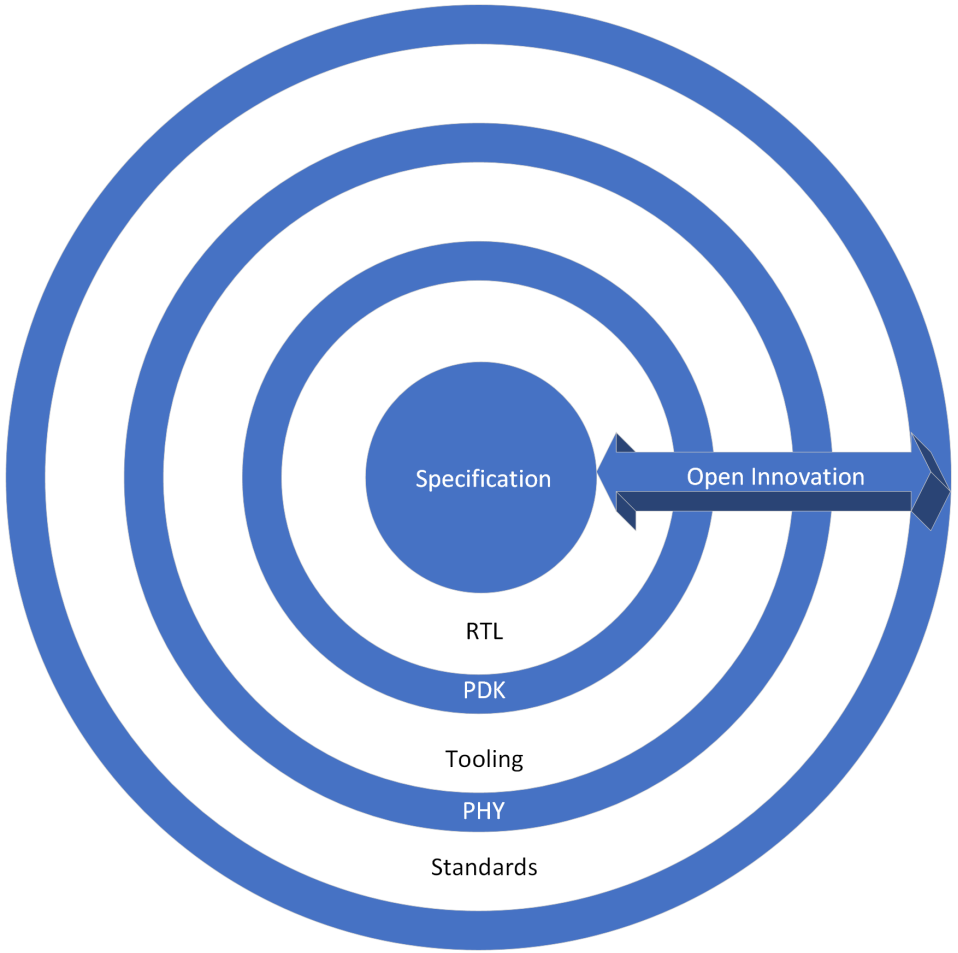
What is Linux Foundation Open Hardware About?

Many Parts to Chip Design

- Instruction Set Architecture
  - Power, RISC-V
- Design Description (RTL)
- Semiconductor (PDK)
- Physical Design
- EDA
- Design Verification
- Test



Many Participants

- Individuals
- Universities
- Foundations
- Industry

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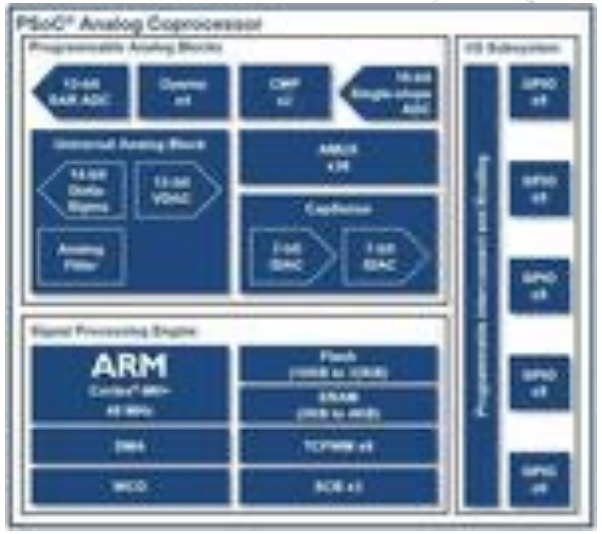
What is a SoC? A System on a Chip

Many pieces

- ‘ A Lego Set
- Unique & Replicated Pieces
- Designed Differently

  -RTL to Gates
  -Custom Circuit Design
  -Memory
  -SERDES
  -Digital
  -Analog

Its complicated.
Ever heard of Kirchoff’s Voltage Law?
How about Maxwell’s Equations?



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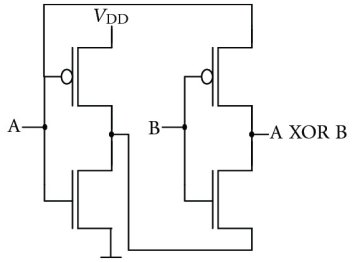
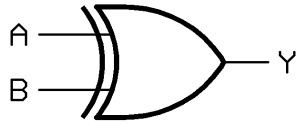
Hiding Complexity -> Increasing Productivity
Making Chip Design Approachable



Transistors

Hand Tuned, Placed, & Routed



Gates

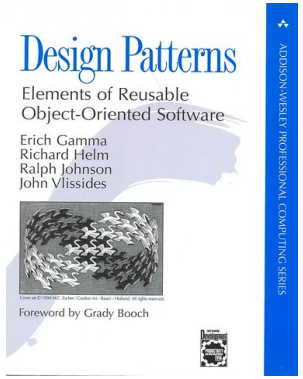
First Level Abstraction

```
// clocked version (not working yet)
always @ (posedge EM_CLK)
begin
    if (!EM_nCE1 && !EM_nWE) begin
        mem[em_addr] <= EM_D;
    end
    if (!EM_nCE1 && !EM_nOE && EM_nWE) begin
        em_outdata <= mem[em_addr];
    end
end

endmodule
```

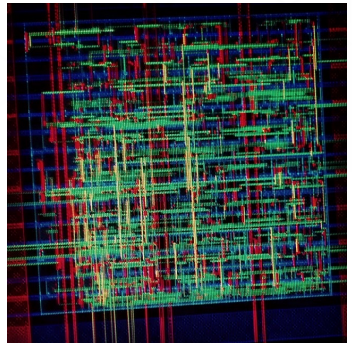
RTL

- H/W Assembler
- Verilog
- VHDL



Software Approach

- Python
- Object Based
- Libraries of Services
- Ease of Reuse
- Integrated Verification



Compilation

- Machine Code
- Layout
- One in Same
- Automate Creation

Accelerating Innovation, Increasing Productivity with Less Resource

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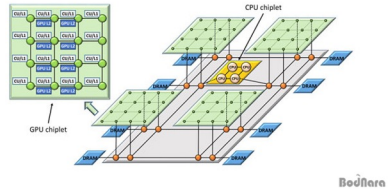
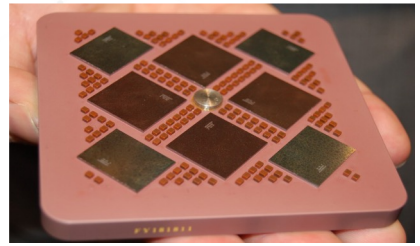
Lego Blocks Enabling Design Interchange

Soft IP

Hard IP

Chiplets





Pick your card to build a winning hand!

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Some Activities of Interest

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AI/ML in Chip Design, EDA, Chip Technology

Open Flywheels

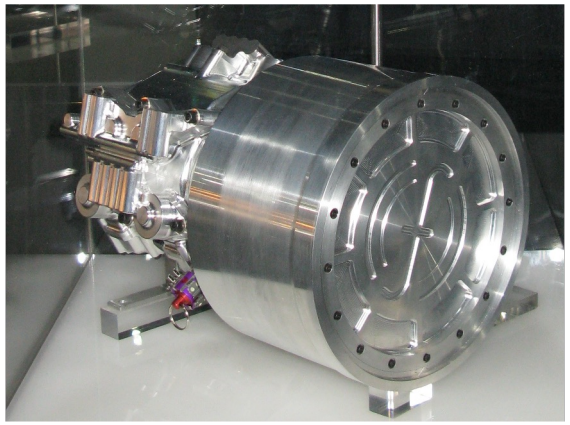
Collaboration is easy!

Ingredients

PDK's
Architecture
EDA

Encased Flywheels

Collaboration is hard!



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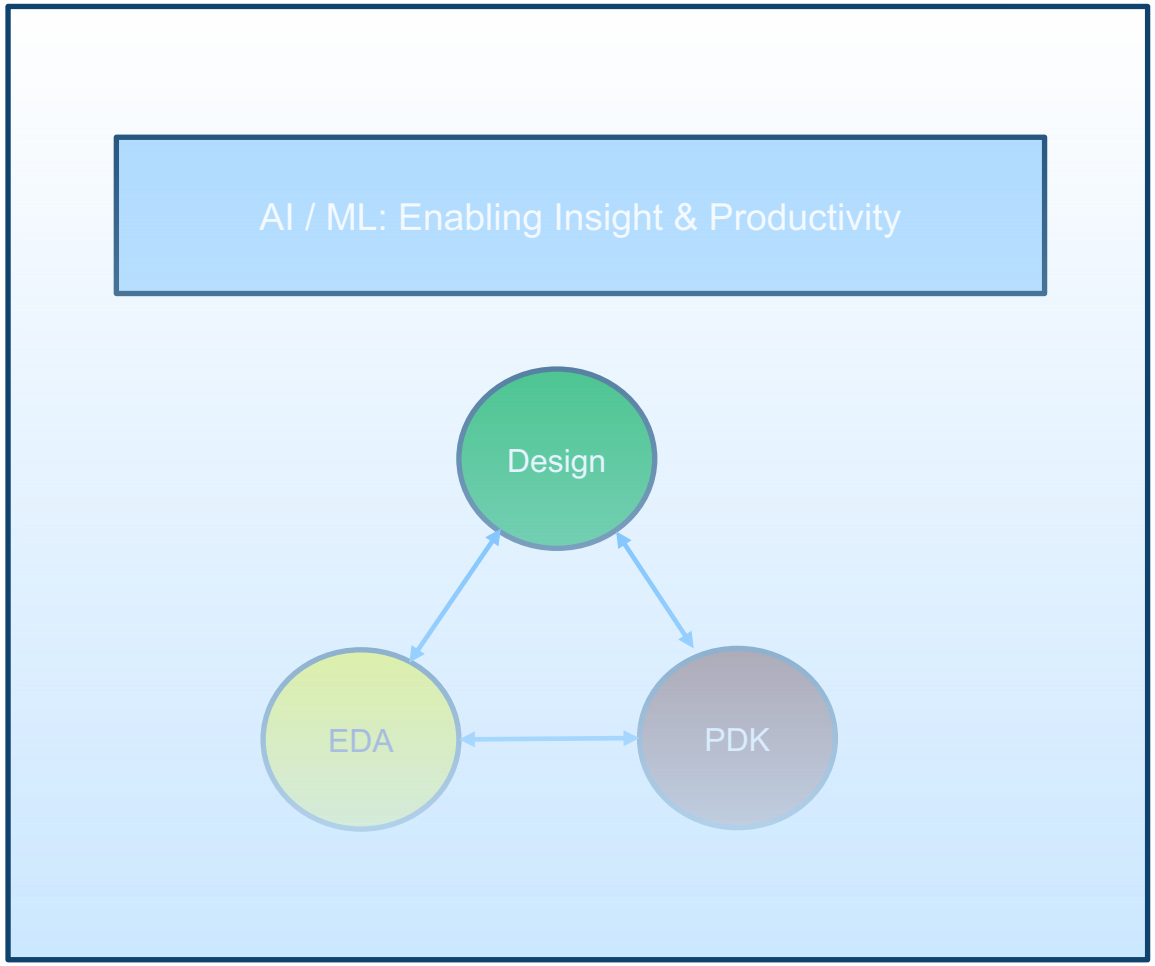
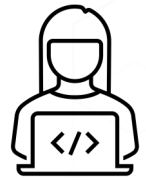
Can we build a collaborative machine learning model to accelerate chip innovation and time to market? Community Data License Agreement can help

What about Chip Design?

The Classic Triad to the New Quad of Hardware Development

Aha!





The ‘New Kid’

The Classic Partners in Crime

What type of box should this system be?
‘Is there an API for that? Why would you want that?’
OpenRoad & ChipFlow ‘open’ potential for EDA & AI based chip design

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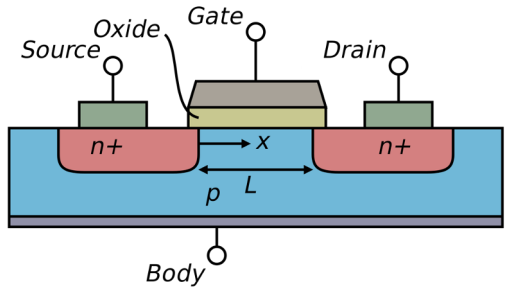
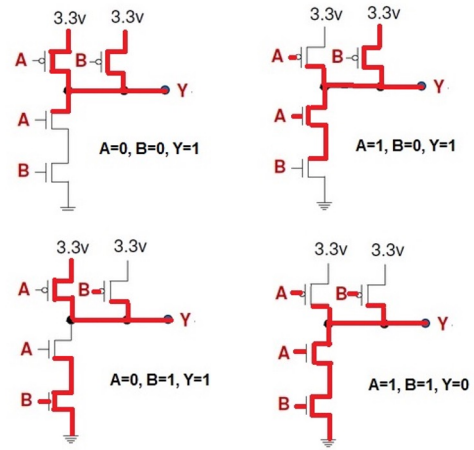
Open Source PDK's

Process Design Kits

- The ingredients for semiconductors
- The foundation of Chip Design





These are being open sourced

-IHP, Global Foundries, Skywater

Enabling Collaboration

Accelerating Innovation

Spice Models
Cell Electric Library Models
Routing Rules
Extraction
LVS/DRC

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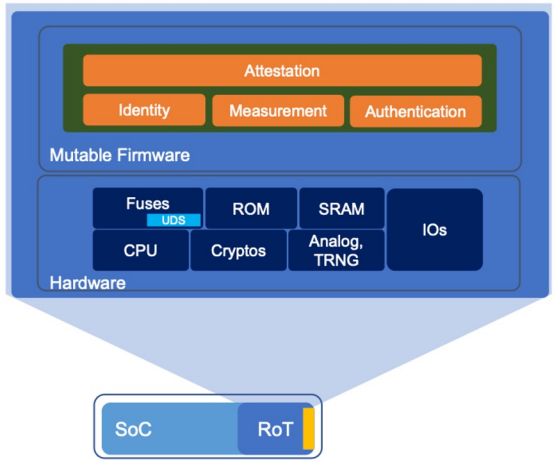
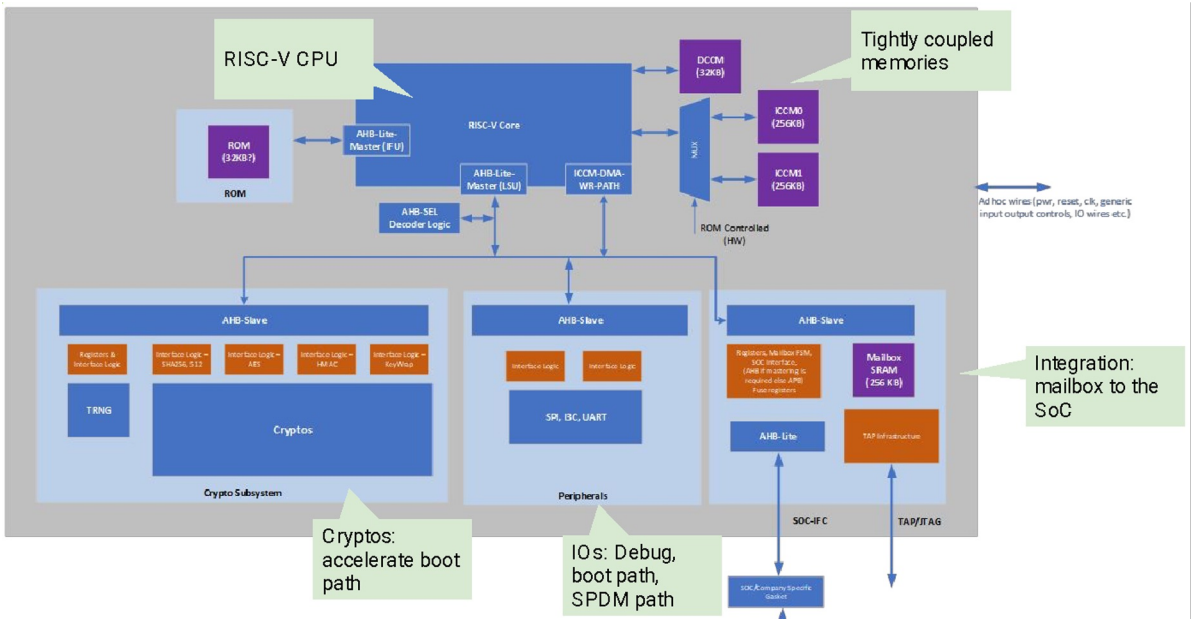
Caliptra: Silicon Root of Trust IP Block

- Open source implementation, Apache 2.0 licensed
- Reusable
- Collaboratively developed
- Incorporates a RISC-V VeeR Core
- Targeted for Datacenters
- Measure, verify, and attest

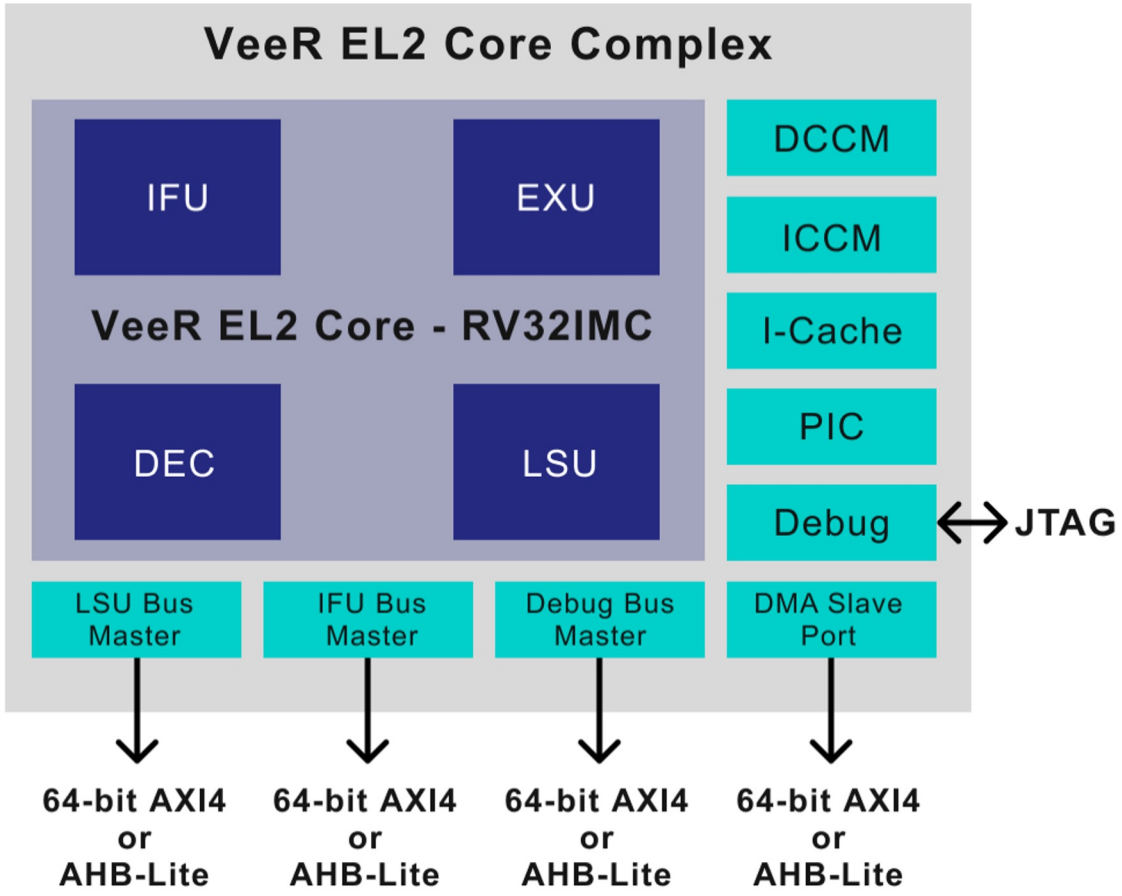


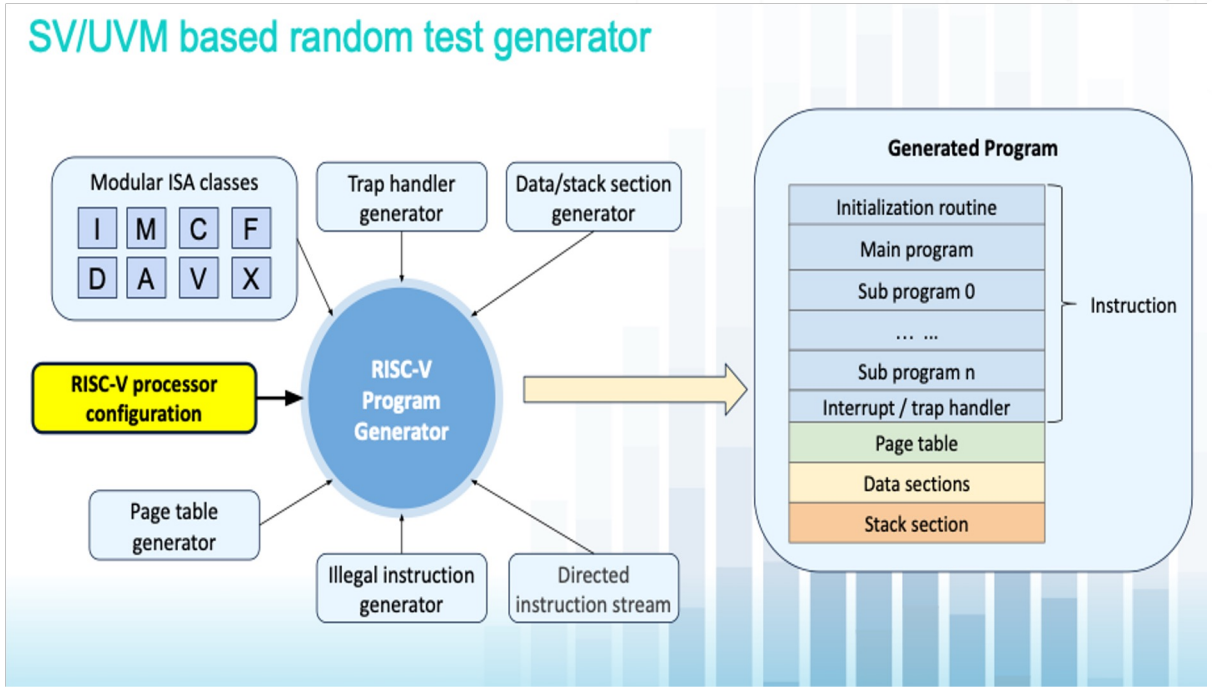


Caliptra 1.0 Now Available
-RTL
-Design Verification
-Firmware

CHIPS ALLIANCE | Caliptra

RISC-V Implementation: VeeR core and Verification Bench





THE F4PGA WORKGROUP

- Established by CHIPS Alliance based on previous work known as SymbiFlow
- F4PGA = FOSS Flow For FPGA
- Goal: drive open source tooling, IP and research efforts for FPGAs
- Groups academia members, industry and FPGA vendors
- Focus on:
    - Open source toolchain for FPGAs (previously known as SymbiFlow)
    - FPGA Interchange Format
    - FPGA Perf Tool
    - FPGA based IP
        - Working on 2 major Design IP contributions

Automating Analog & Digital Implementation with Open Source EDA

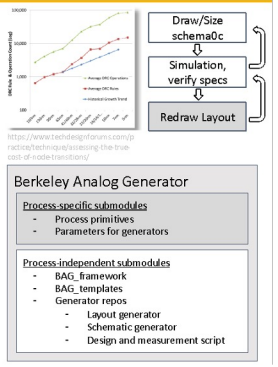
Analog Generators with Berkeley Analog Generator (BAG)

Analog Circuit Design Issues

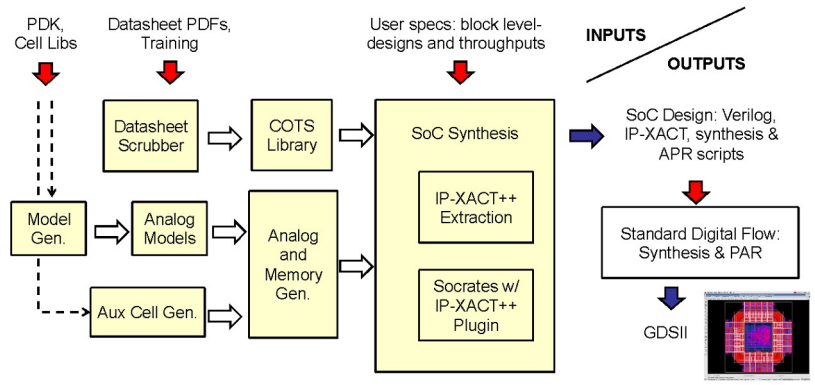
- Advanced technologies are becoming more and more complicated
- Analog circuit design is not agile in nature

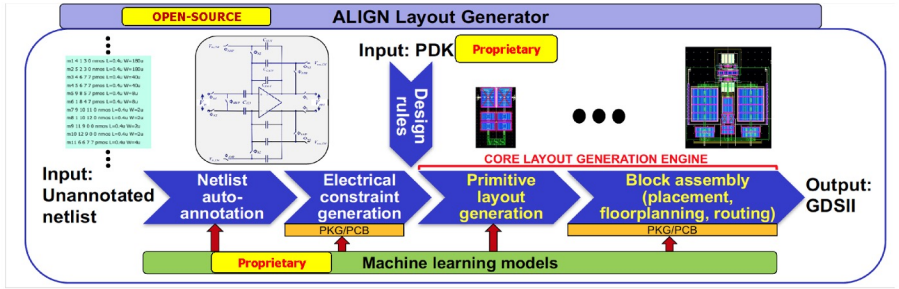
Berkeley Analog Generator

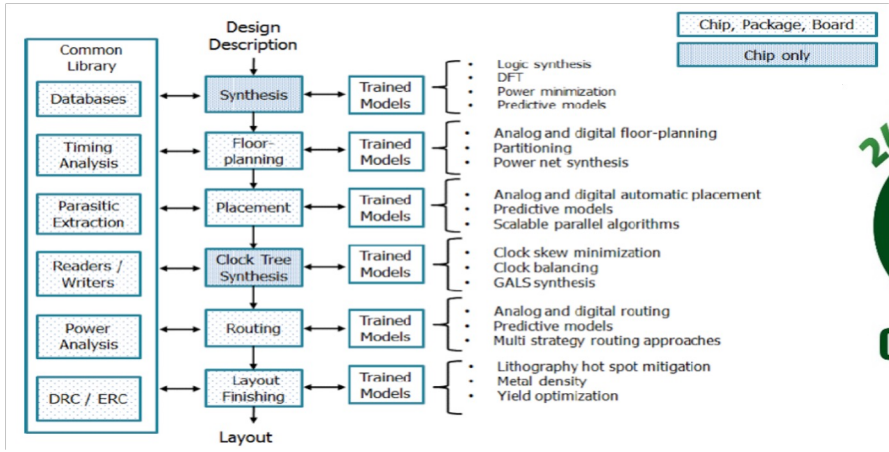
- Provides an interface between python and CAD tools
- Contains process configuration files, schematic generators, layout generators
- Call functions to generate schematic, layout, run extraction, simulation and iterate



FASoC Tools Family and Flowchart







UNIVERSITY OF MINNESOTA
Driven to Discover®

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24h OpenROAD

Gaining Confidence in *Open* Design with Real Silicon

Intel's University Shuttle

intel foundry services

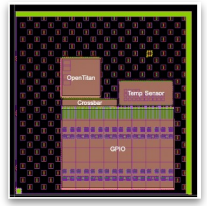
Start of Skywater's Open MPW Program

DARPA IDEA Program

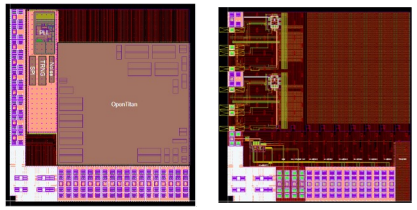
Nanofab. Accelerator program w. NIST

Globalfoundries Open MPW Program

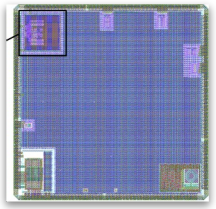
Intel 16-nm



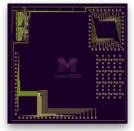
Intel 16-nm



GF 12-nm

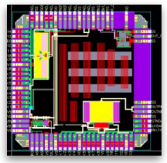


GF 180

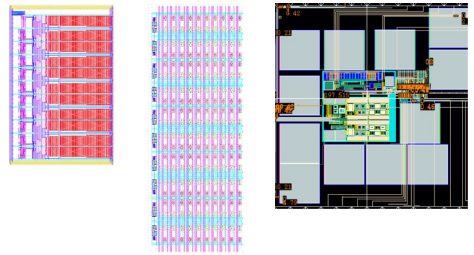


MPW0

GF 180

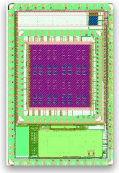


Project w. Fitbit

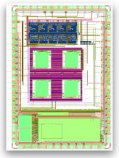


NIST's Nanofabrication Tapeout

SKY130



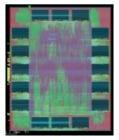
MPW1 Dec



MPW2 …. Jun

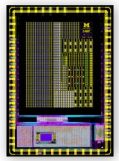
MPW3 Aug

Oct



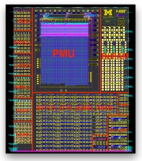
MPW4 Dec

1st TO



MPW5 Feb

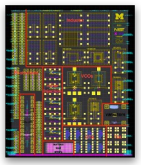
2nd TO



Apr

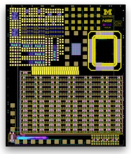
MPW6 Jun

3rd TO

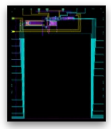


MPW7 Aug

4th TO



MPW8 Oct



Dec

Feb

Apr

Jun

End of 2020

2021

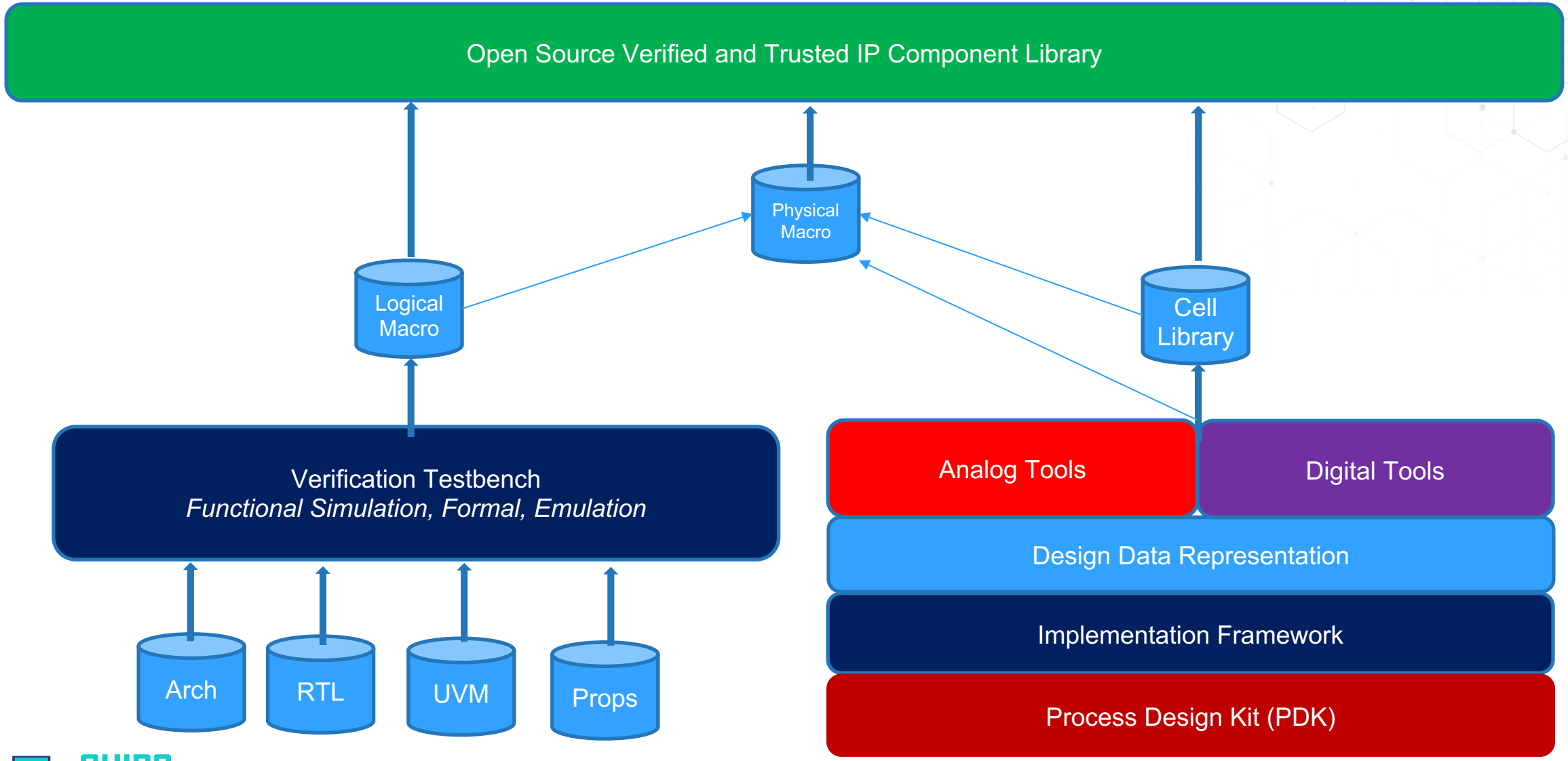
2022

Feb 24th

May 28th

2024

Open Hardware Design with Catalog of Trusted Ingredients



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Verification and Implementation Platforms

Open Hardware Mini-Summit Talk Schedule

Time	Speaker	Topic Area
13:30 - 14:00	Rob Mains General Manager, CHIPS Alliance	Welcome / Opening Remarks
14:00 - 14:30	Andrea Gallo VP Technology, RISC-V	RISC-V: Getting Involved, Latest Advancements
14:30 - 15:00	Itai Yarom VP, Strategic Alliances, MIPS	Accelerating collaboration in the automotive industry by using open-source software and open-source ISA (RISC-V)
15:00-15:30	Daniel Mueller-Gritschneder Johannes Geier Professor, TU Wien	Open Source Simulators for Pre-Silicon Validation of Safety-critical RISC-V System-on-chip
15:30 - 16:00	Break	
16:00 - 16:30	Karol Gugala Engineering Manager, Antmicro	Making VeeR EL2 Caliptra 2.0-ready: enhanced functionalities, verification and documentation
16:30 - 17:00	Christoph Sandner Senior Principal Engineer, Infineon	Value and Opportunities in Open Source for Circuit Design
17:00 - 17:30	Rob Taylor Chief Strategy Officer, ChipFlow	Open Source IC design for Automotive: Real World Experience
17:30	Event End	

CHIPS ALLIANCE

Innovation by Collaboration: Open Hardware Development

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