RISC-V opportunity, innovation, and collaboration igniting adoption

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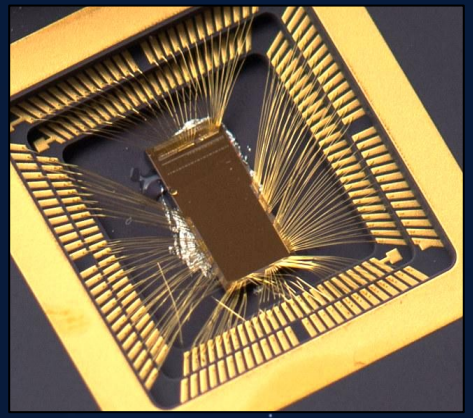
RISC-V is the industry standard ISA that **expands opportunity**

RISC-V®

Global standards are a catalyst to accelerate technical innovation

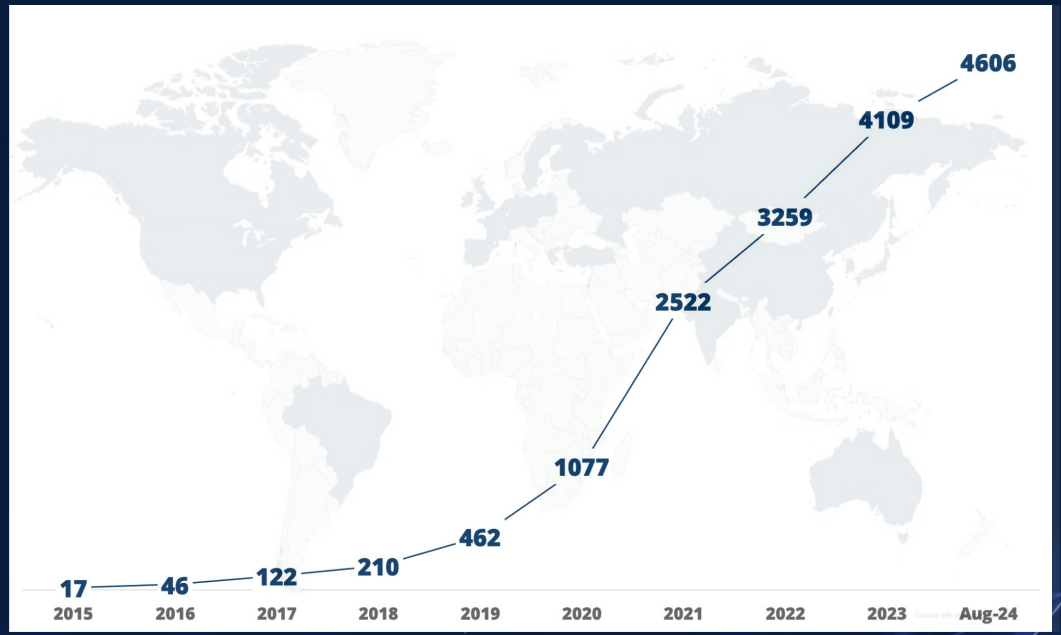
Standards have been critical to technology innovation, adoption, and growth for decades

Standards create access to opportunities and spur growth for a wide range of stakeholders



RISC-V is a standards-defined Instruction Set Architecture developed by a global community

More than 4,600 RISC-V Members across 70 Countries



Aug 2024 update

110 Chip
SoC, IP, FPGA

4 Systems
ODM, OEM

3 I/O
Memory, network, storage

18 Industry
Cloud, mobile, HPC, ML, automotive

21 Services
Fab, design services

183 Research
Universities, Labs, other alliances

52 Software
Dev tools, firmware, OS

>4200 Individuals
RISC-V engineers and advocates

RISC-V membership up 28% in 2023

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40

New technical specifications ratified in the past **two years** including 123 ratified extensions

75

Technical Working Groups collaborating together

123

Extensions

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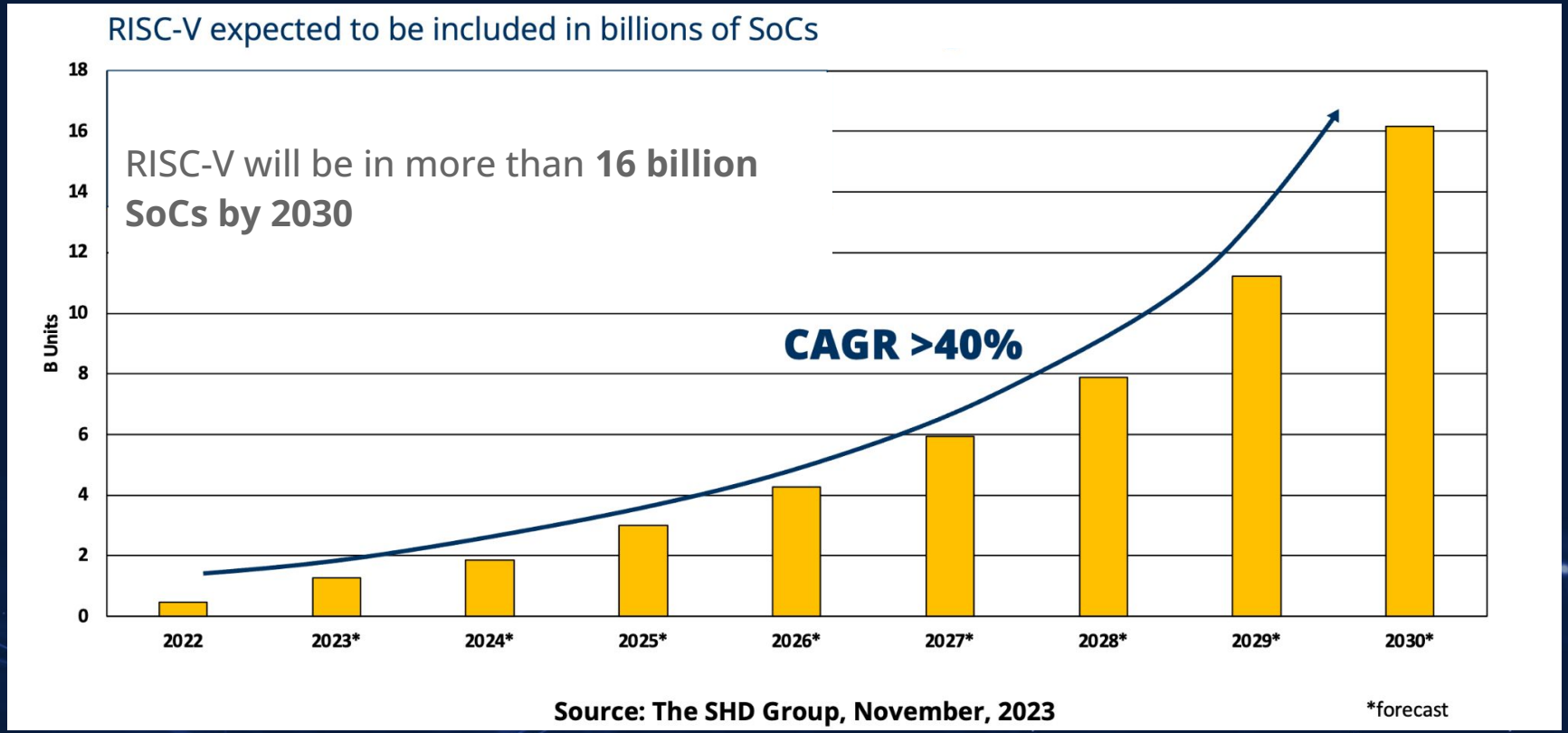
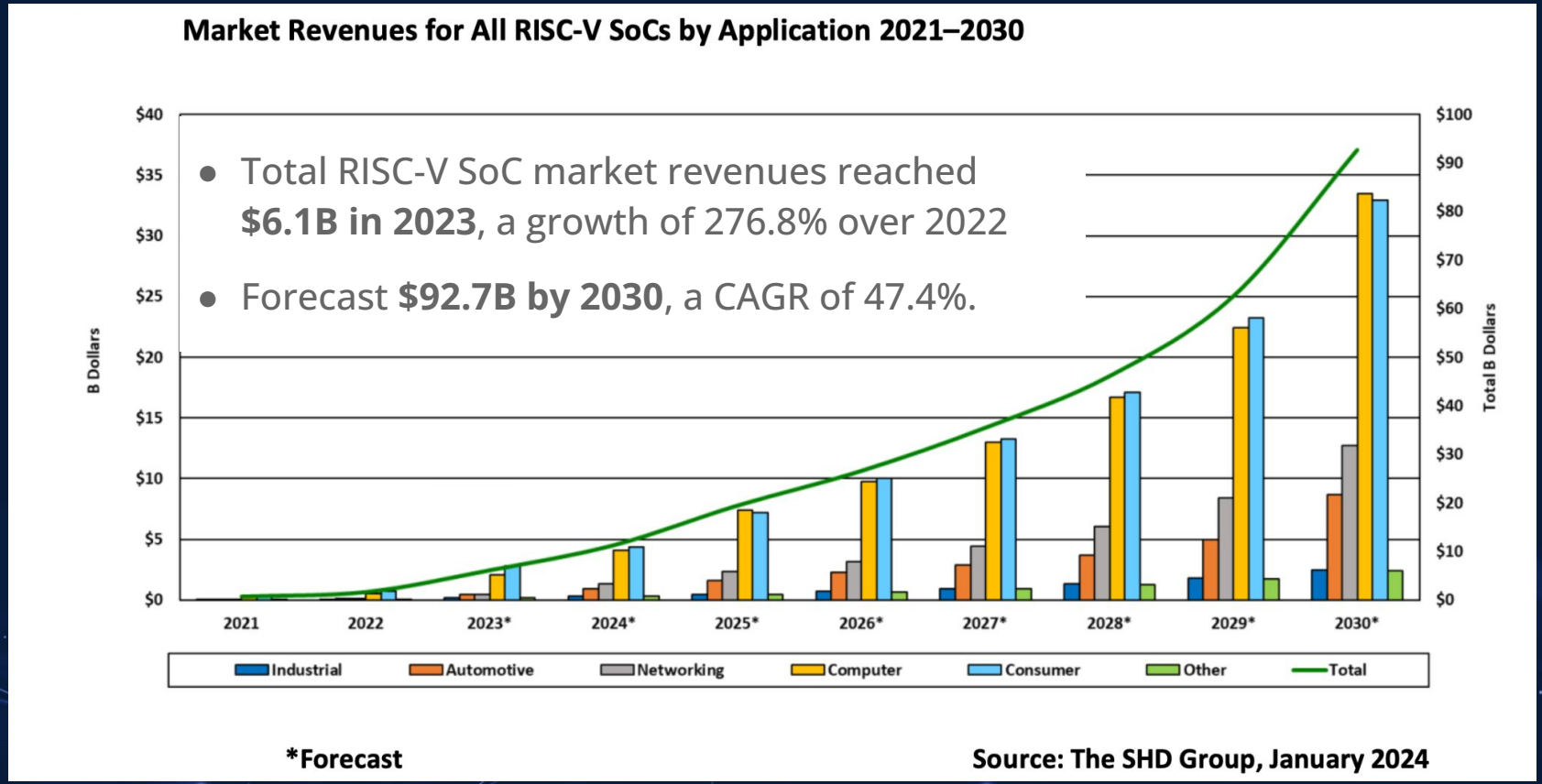
Incredible Market Potential

RISC-V is Inevitable

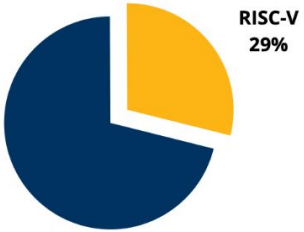


RISC-V market revenues forecast $92.7B by 2030



Market Share Projections for RISC-V in 2030

Wearables
MCU



TAM: 2.6B units

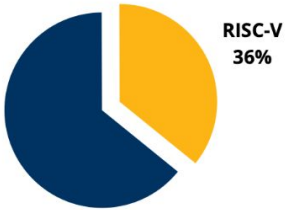
Computing
Notebooks

TAM: 2.7B units

Communications
5G Infrastructure

TAM: 1.8B units

Consumer
AI Acceleration



TAM: 6.4B units

Industrial
Smart Grid

TAM: 670M units

Automotive
AI Acceleration

TAM: 260M units

Based on projected SoC volumes

Source: The SHD Group, November, 2023

the SHDgroup

The technical foundation for lasting success

Countries

- Tech sovereignty
- Accelerate local innovation and talent
- Incubate technology ecosystem from research to industry
- Access worldwide market

Multinationals

- Control strategic roadmap
- New opportunities for innovation and influence
- Growth business models
- Avoid vendor lock-in

Researchers

- Collaborative ISA thought leadership
- Enables innovative research
- Access global RISC-V research network
- Tech transfer addressing real world applications

Startups

- Supercharge hardware and software co-design
- Accelerate strategic roadmap in greenfield applications
- Collaboration partners

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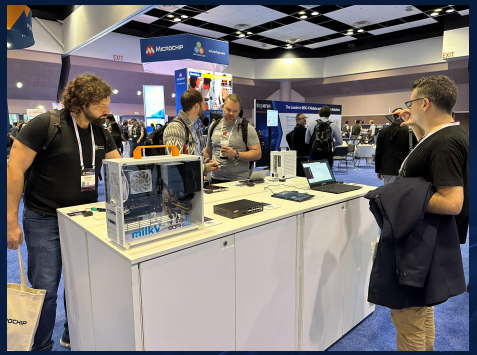
RISC-V Events



Discover the worldwide RISC-V Ecosystem at RISC-V Summits and events

Major RISC-V Summits in 2024

EU

June 24-28

722 delegates + exhibitors
RISC-V 101 + 1st Hackathon

https://riscv-europe.org/

China

July 21-23

3,000 in person delegates
10,000 remote participants

https://riscv-summit-china.com/en/

North America

October 21-23

1,070 attendees in 2023
RISC-V 101 + 2nd Hackathon

https://riscv.org/event/risc-v-summit-north-america-2024/

There are many RISC-V days around the world, check out the nearest location!

RISC-V

SUMMIT EU

JUNE 24 – 28 | MUNICH 2024

Top talks on AI and HPC

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

openchip

semidynamics

AXELERA ARTIFICIAL INTELLIGENCE

Top talks on Functional Safety, Real Time, Automotive

THALES

BOSCH

Infineon technologies

ETH zürich

QUINTAURIS

https://riscv-europe.org/

RISC-V

第4届 2024

RISC-V 中国峰会

RISC-V Summit China

BOSC and University of Chinese Academy Sciences (UCAS) launched the one student one chip program in 2019

- First full RV64 CPU in 4 months
- 7,000 students so far, 13 chips taped out in 2023
- XiangShan NanHu open source RISC-V processor and laptop with AMD RX550 discrete GPU on github

Full open source EDA on github

DC-ROMA RISC-V Laptop II

- Octa-core RISC-V CPU up to 2GHz
- Ubuntu 23.10 pre-installed
- SpacemiT K1 SoC 256-bit RVV 1.0 vector and NPU

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SUMMIT
October 22-23, 2024 · Santa Clara, CA
#RISCVEverywhere #RISCVSummit
RISC-V 101 and 2nd RISC-V Hackathon on October 21

Brazil joined as a Premier Member in 2024

250

Engineers to train on chip design

$150M

Investment in RISC-V accelerator

25

AI Infrastructure Projects over 5 years

https://riscv.org/blog/2024/09/advancing-ai-the-brazilian-way-fostering-innovation-through-collaboration-and-open-standards/

Invest locally
Engage globally

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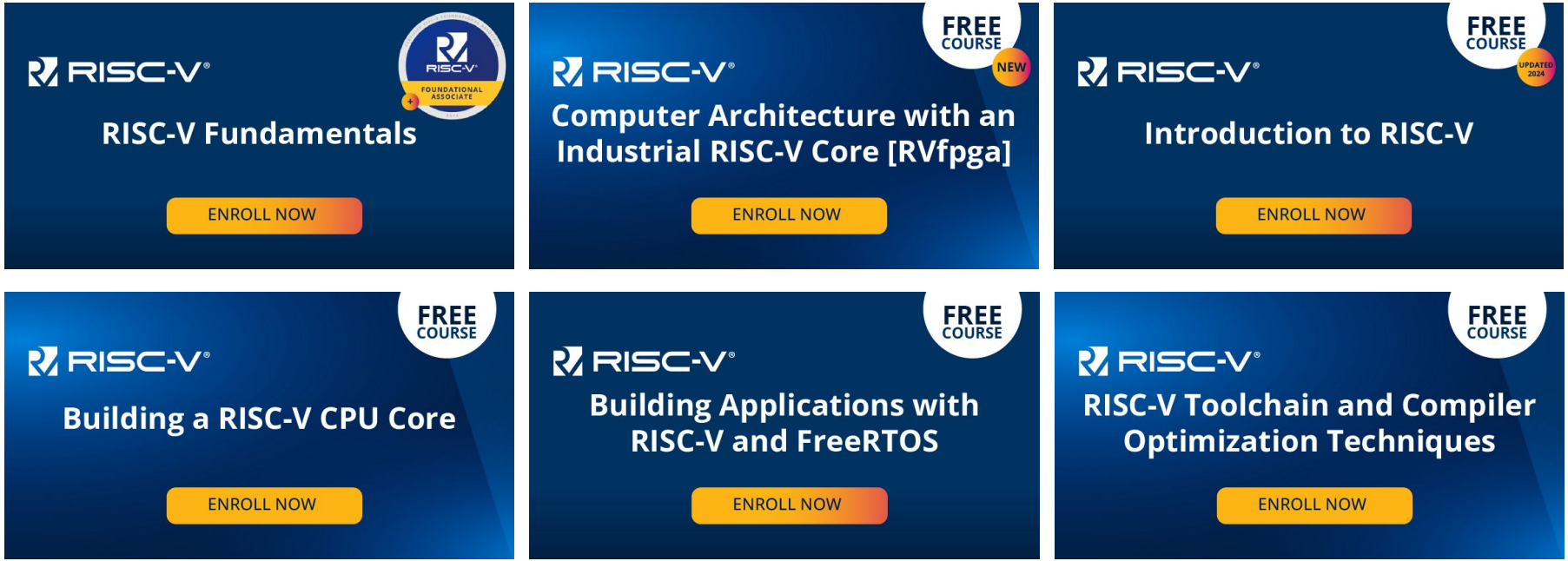
Engage in RISC-V
1 - Learn

RISC-V Online Learning



https://riscv.org/certifications-and-courses/

RISC-V Courses & RVFA Certification

- ★ FREE courses including Building a RISC-V CPU Core and Introduction to RISC-V
- ★ RISC-V Foundational Associate Certification and RISC-V Fundamentals to train new employees
- ★ Members receive a 30% discount on training and certification

The certification is also available in Chinese.

The course is also available in Chinese.

Reach out to learn@riscv.org for more information

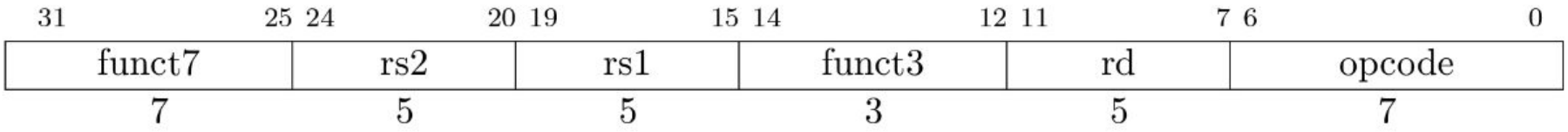
GET RISC-V CERTIFIED!

RISC-V FOUNDATIONAL ASSOCIATE CERTIFICATION

(RVFA)

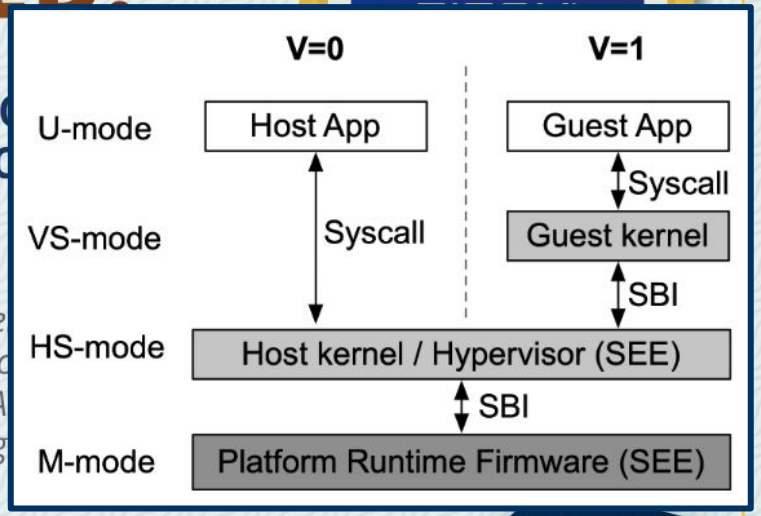
Companies utilizing RISC-V are actively seeking skilled programmers and designers who grasp the RISC-V architecture and are also well-versed in its intricate specifications. Are you ready to meet this demand? Elevate your skills and get qualified now!

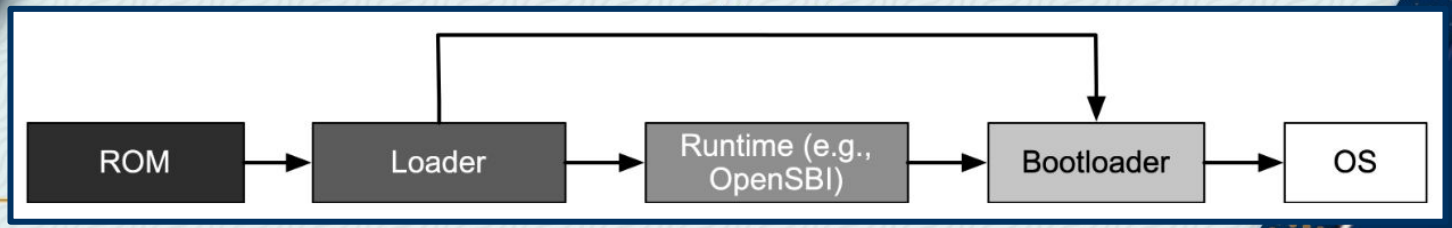
Get prepared ★★★ 2024 **Get qualified**



Structure of the generic R-type instruction

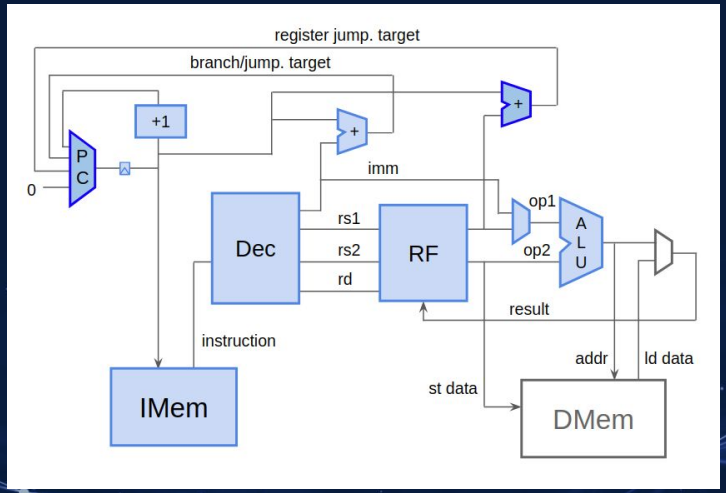
```
1    .text
2    .align 2
3    .globl main
4
5    main:
6        addi t0, x0, 0x5    # Initialize t0 to 5
7        addi t1, x0, 0x0    # Initialize t1 to 0
8    loop:
9        add  t1, t1, t0     # Increment t1 by t0
10       addi t0, t0, -1     # Decrement t0 by 1
11       bnez t0, loop       # If t0 is not zero, go to
12       lui  t0, 0x1        # Set t0 to point to addres
13       addi t0, t0, 0x100  # Add 0x100 to t0, to make
14       sw   t1, 0(t0)      # Store the result in 0x110
```

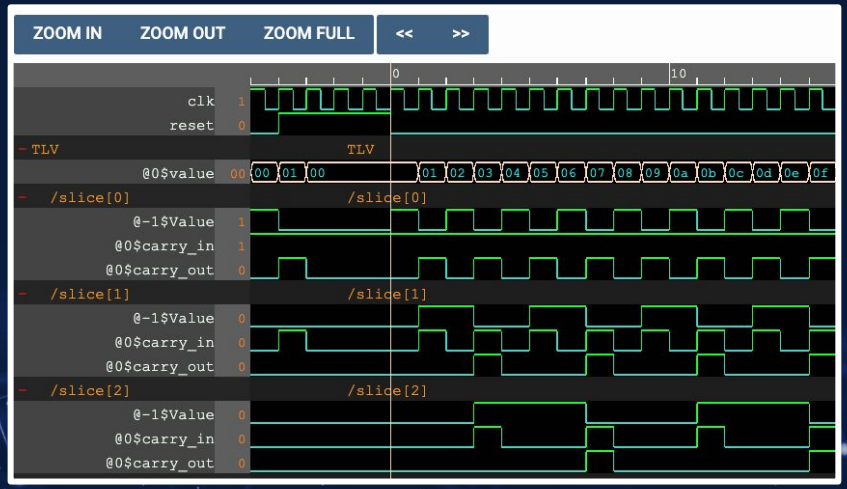




LFD111x - Building a RISC-V CPU Core

Create a RISC-V CPU with modern open source circuit design tools, methodologies, and microarchitecture, all from your browser





https://www.edx.org/learn/design/the-linux-foundation-building-a-risc-v-cpu-core

Engage in RISC-V
2 - Develop

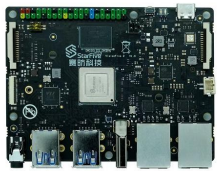
A robust software ecosystem is essential for RISC-V adoption

- Enable upstream software on ratified RISC-V ISA and extensions
- Contribute RISC-V hardware to strategic software projects
- Accelerate developer journey to RISC-V

Enabling Developers with Hardware and Cloud Compute

RISC-V DEVELOPER BOARDS

RISC-V LAB PARTNER



10x ENGINEERS

PLCT Lab

In Process

Oregon State University

RISC-V®

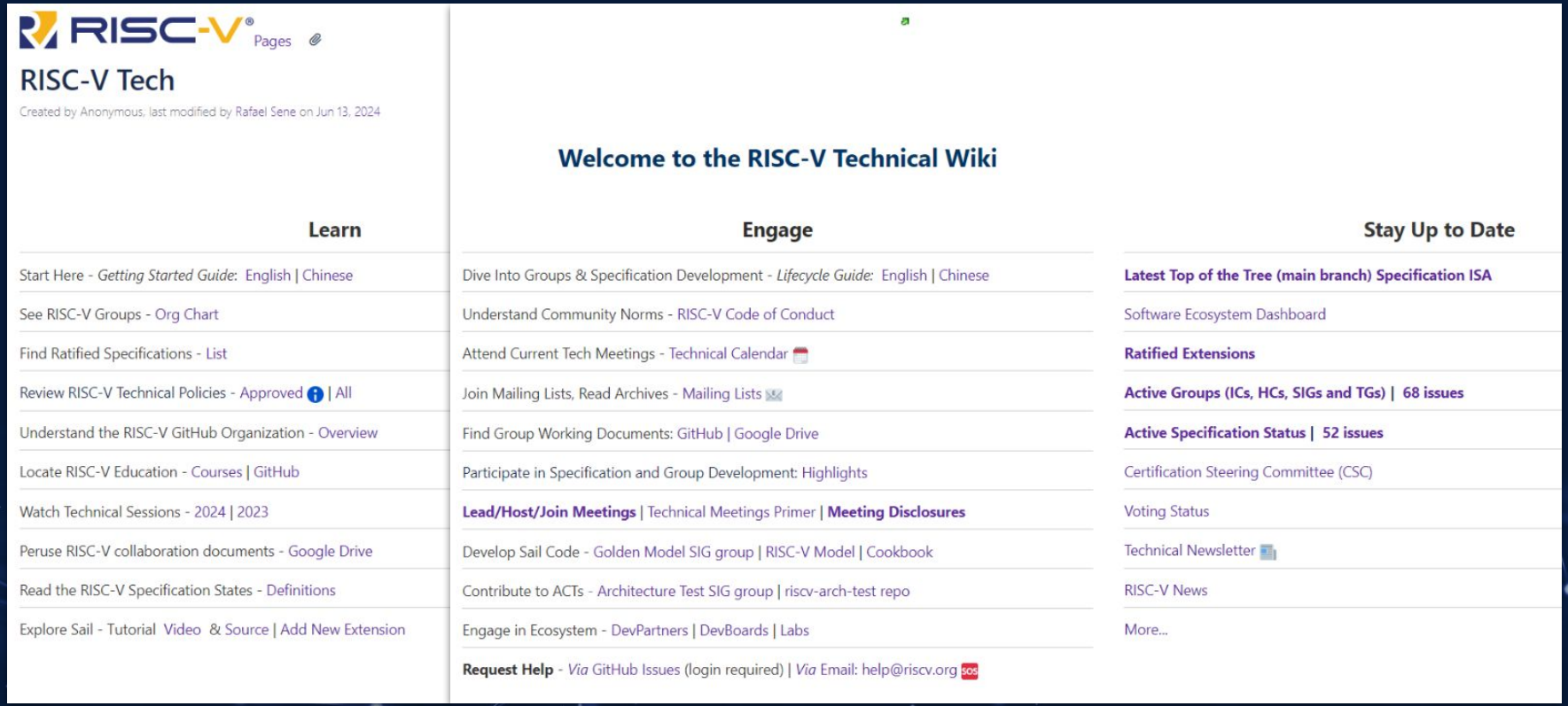
Building the strongest ecosystem

Funding of $7.8B

landscape.riscv.org

Engage in RISC-V
3 - Contribute

The First Place to Look - the RISC-V wiki!



RISC-V® Pages

RISC-V Tech

Created by Anonymous, last modified by Rafael Sene on Jun 13, 2024

Welcome to the RISC-V Technical Wiki

Learn	Engage	Stay Up to Date
Start Here - *Getting Started Guide*: English | Chinese	Dive Into Groups & Specification Development - *Lifecycle Guide*: English | Chinese	**Latest Top of the Tree (main branch) Specification ISA**
See RISC-V Groups - Org Chart	Understand Community Norms - RISC-V Code of Conduct	Software Ecosystem Dashboard
Find Ratified Specifications - List	Attend Current Tech Meetings - Technical Calendar	**Ratified Extensions**
Review RISC-V Technical Policies - Approved | All	Join Mailing Lists, Read Archives - Mailing Lists	**Active Groups (ICs, HCs, SIGs and TGs) | 68 issues**
Understand the RISC-V GitHub Organization - Overview	Find Group Working Documents: GitHub | Google Drive	**Active Specification Status | 52 issues**
Locate RISC-V Education - Courses | GitHub	Participate in Specification and Group Development: Highlights	Certification Steering Committee (CSC)
Watch Technical Sessions - 2024 | 2023	**Lead/Host/Join Meetings** | Technical Meetings Primer | **Meeting Disclosures**	Voting Status
Peruse RISC-V collaboration documents - Google Drive	Develop Sail Code - Golden Model SIG group | RISC-V Model | Cookbook	Technical Newsletter
Read the RISC-V Specification States - Definitions	Contribute to ACTs - Architecture Test SIG group | riscv-arch-test repo	RISC-V News
Explore Sail - Tutorial Video & Source | Add New Extension	Engage in Ecosystem - DevPartners | DevBoards | Labs	More...
	Request Help - *Via* GitHub Issues (login required) | *Via* Email: help@riscv.org	

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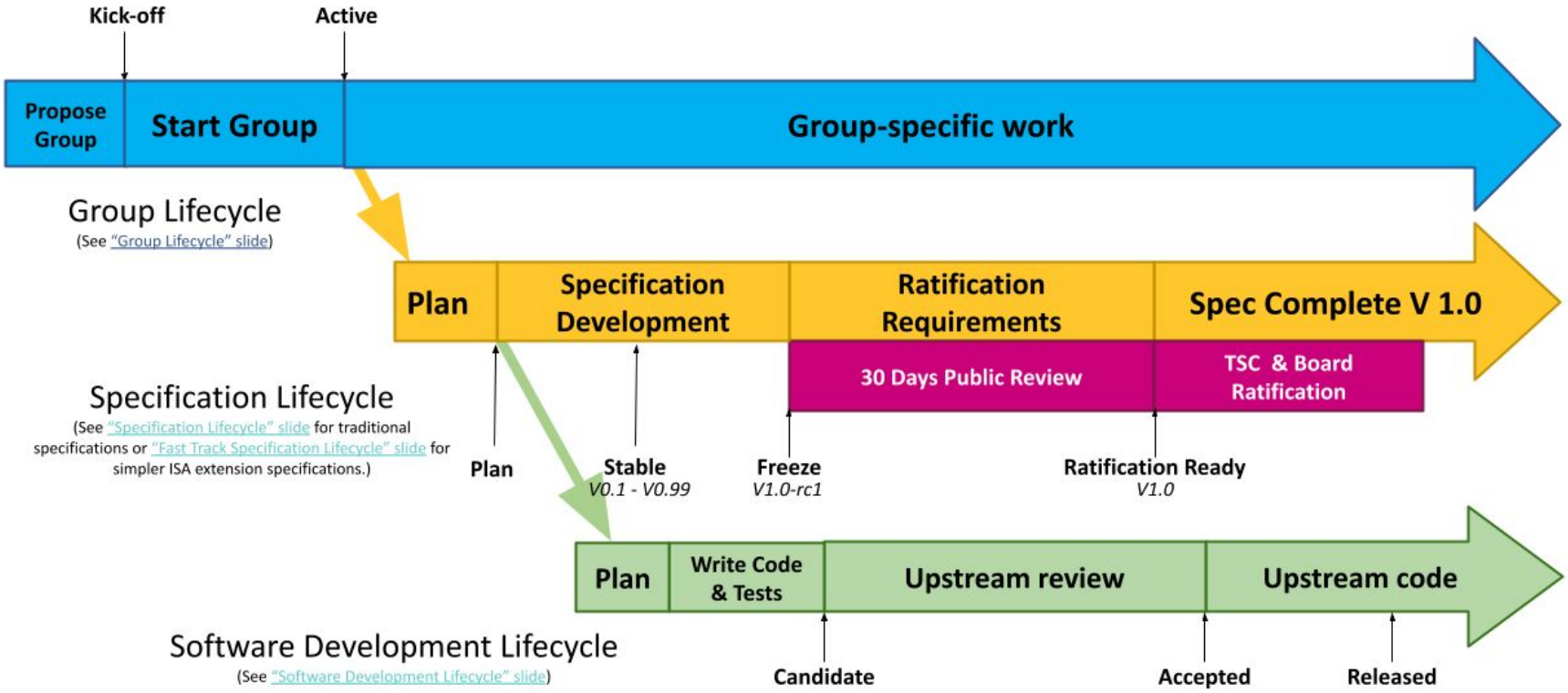
We produce specifications, models and tests



RISC-V ISA is our core work

Adding extensions to the basic ISA

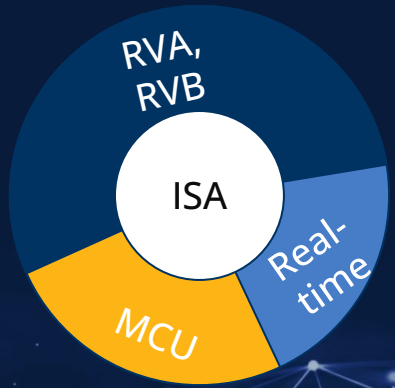
I — Base integer instruction set
M — Integer multiplication and division
A — Atomic instructions
F — Single precision floating point
D — Double precision floating point
Q — Quad precision floating point
C — Compressed instructions
V — Vector/SIMD operations
P — Packed SIMD/vector instructions
N — User level interrupts
S — Supervisor mode
U — User mode
H — Hypervisor mode
B — Bit manipulation instructions

J — Dynamically translated languages support
T — Transactional memory support
L — Decimal floating point
G — Additional general instructions
Zba — Address generation instructions
Zbb — Basic bit-manipulation instructions
Zbc — Carry-less multiply instructions
Zbs — Single bit instructions
Zbt — Ternary bit manipulation instructions
Zfh — Half precision floating point
Zvfh — Half precision vector floating point
Zvlsseg — Vector segment loads and stores

Combining extensions into profiles

RVA22U64
M, A, F, D, C, Zicsr, Zicntr, Ziccif, Ziccrse, Ziccamoa, Zicclsm, Za64rs, Zihpm, Zba, Zbb, Zbs, Zic64b, Zicbom, Zicbop, Zicboz, Zfhmin, Zkt

RVA22S64
Zifencei, Ss1p12, Svbare, Sv39, Svade, Ssccptr, Sstvecd, Sstvala, Sscounterenw, Svpbmt, Svinval



RVM23U32
RV32I, M, Zba, Zbb, Zbs, Zicond, Zihintpause, Zihintntl, Zce, Zicbop, Zimop

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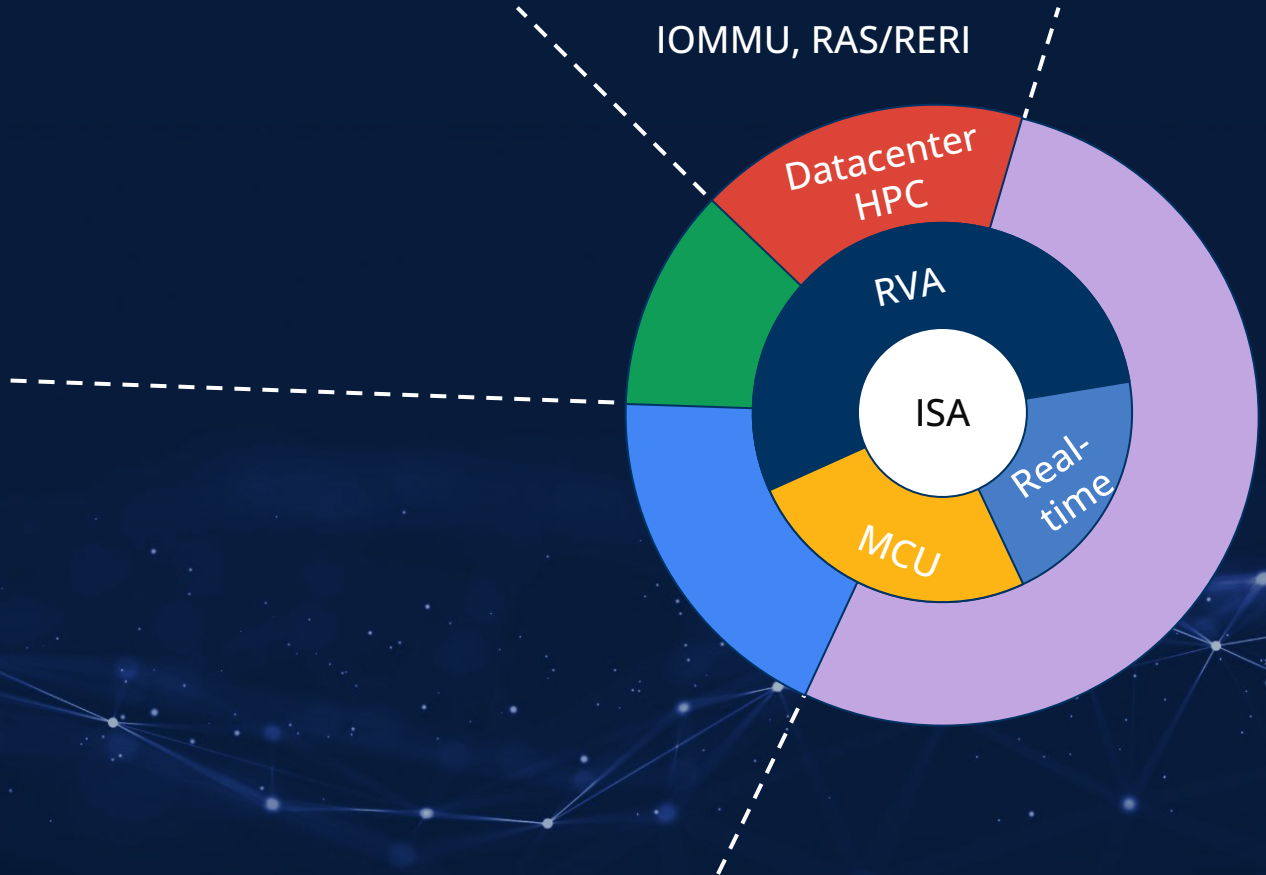
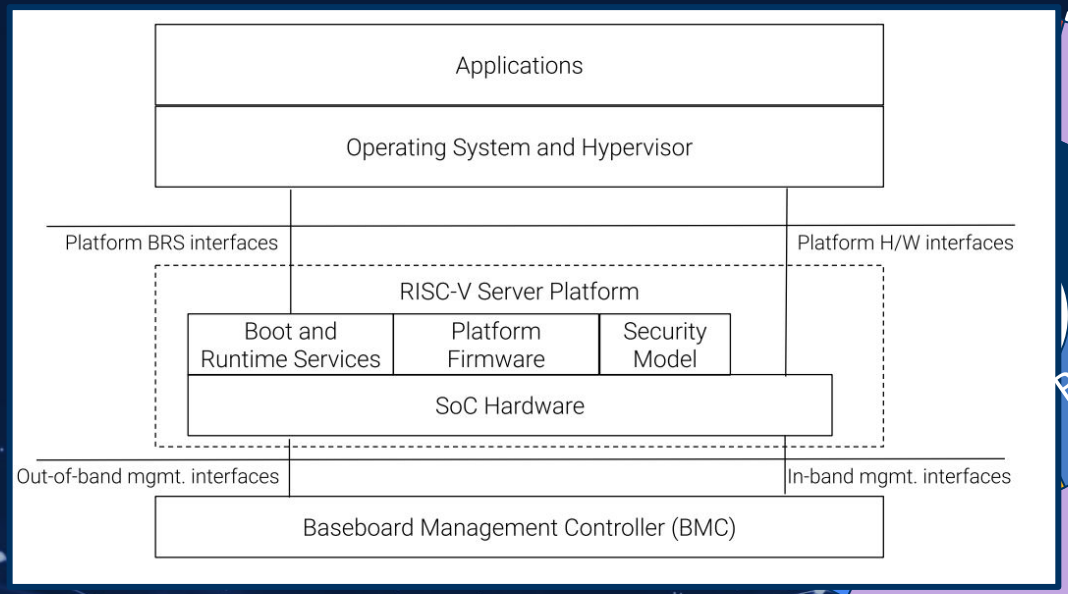
Platforms



Server SoC and Platform

IOMMU, RAS/RERI



Real-time

Server SoC

- Clocks and Timers
- Interrupt Controllers
- IOMMU
- PCIe subsystem
- Reliability, Availability, and Serviceability
- Quality of Service
- Performance monitoring
- Security

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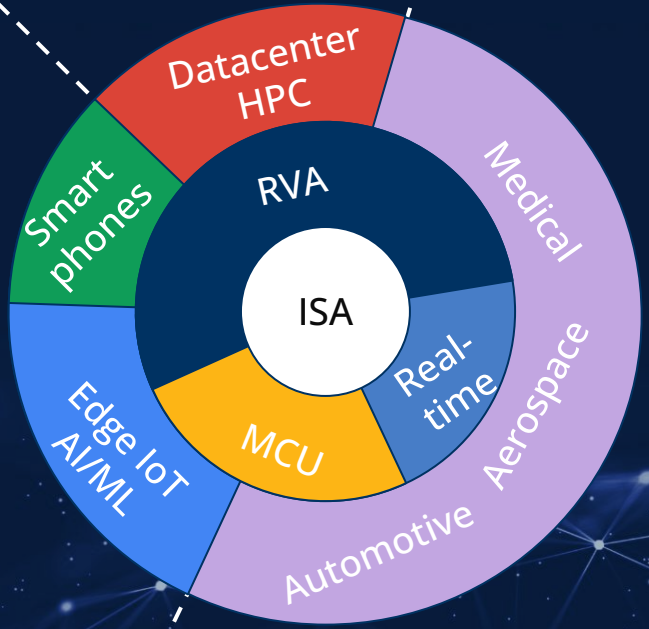
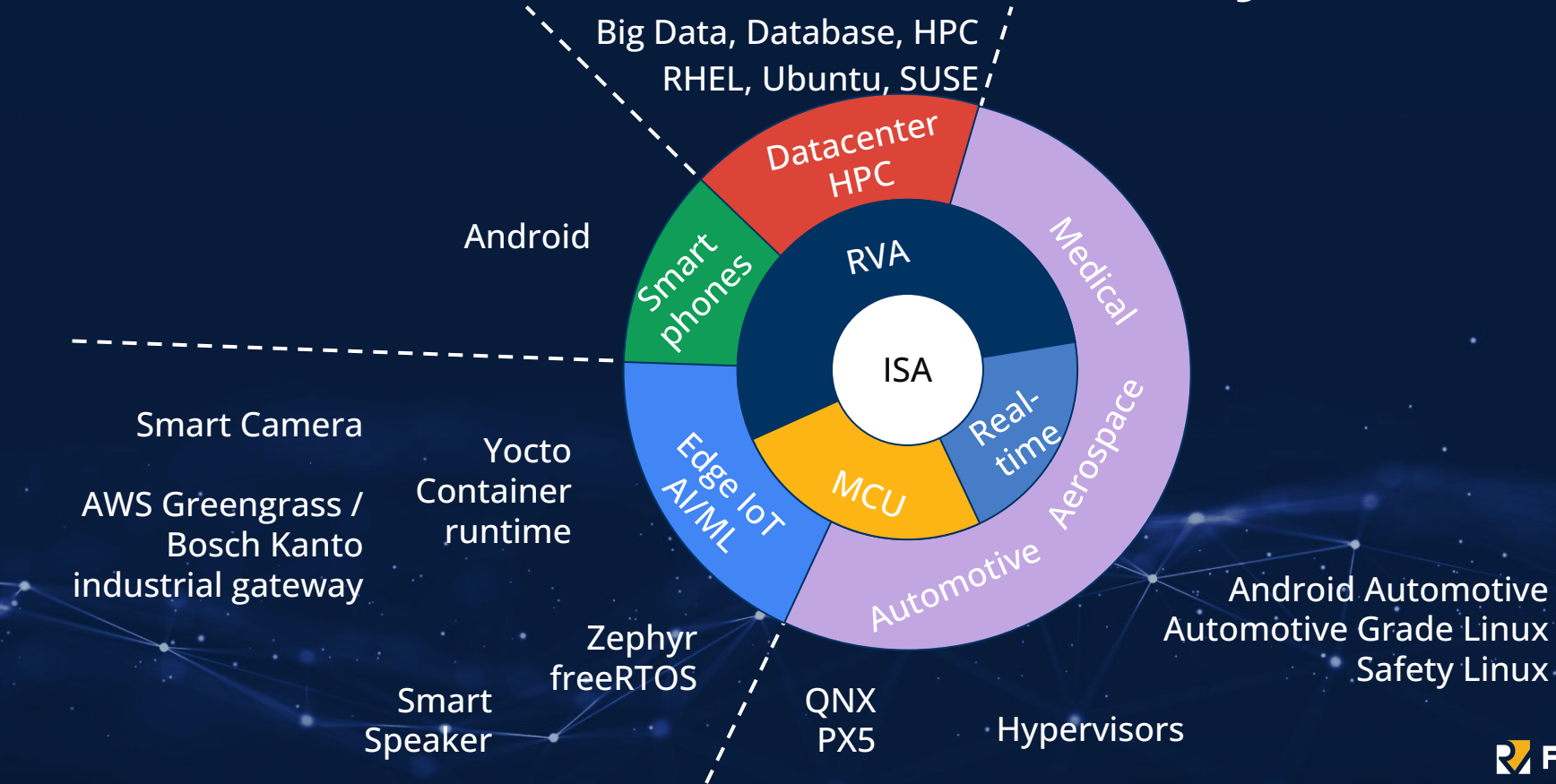
Platforms and industry verticals



Platforms and the software ecosystem



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+

your innovation

RISC-V expands opportunity

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Thank you