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# Porting Android onto RISC-V

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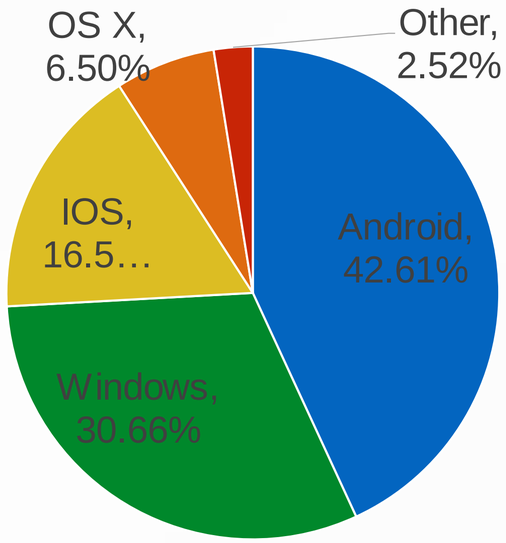
Oct. 12th, 2021

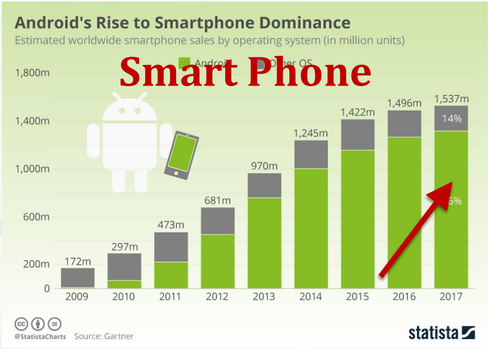
# Android is taking a lot of Market Share…

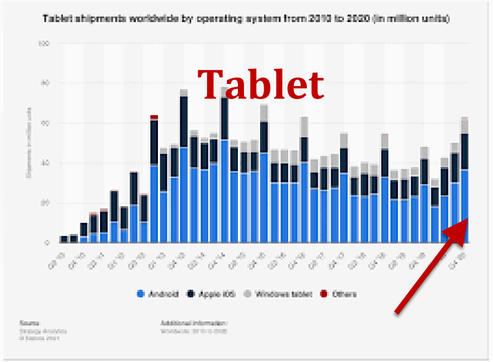
Most popular OS in the world(42.61% on all platforms)

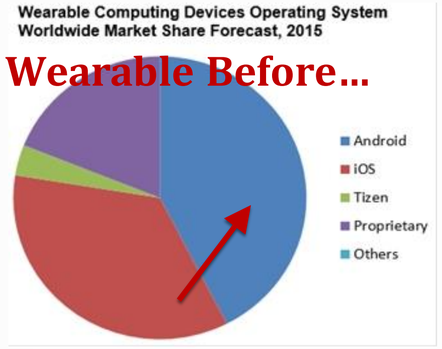
and 2.5 billion active users spread over 190 countries

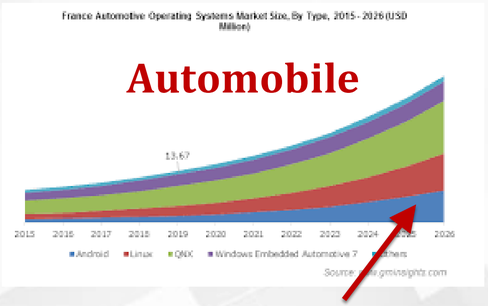


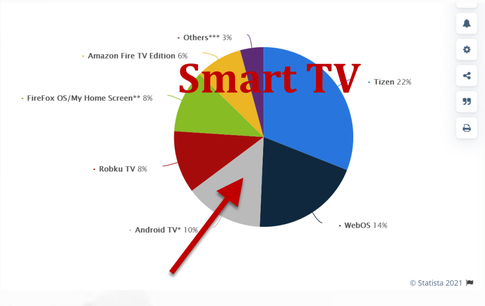

Operating System Market Share Worldwide - August 2021

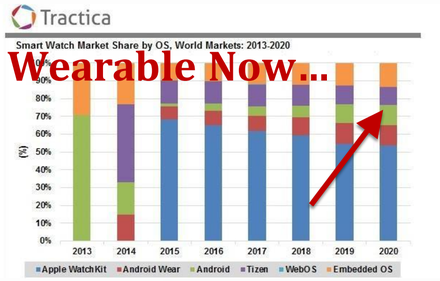



Widely used in mobile device, automotive, smart TV, wearables markets and etc.

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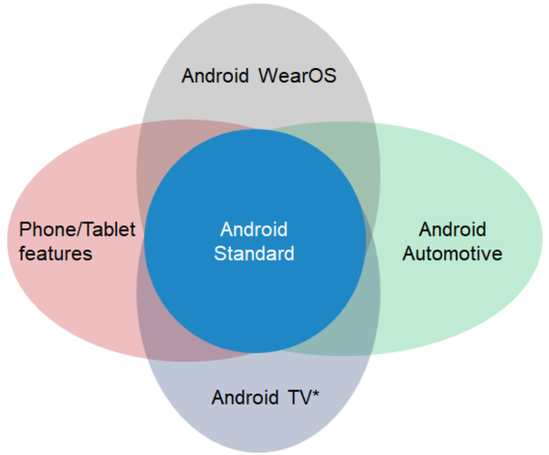
# Android Ecosystem




## Android ecosystem

- SDK
- NDK
- VNDK
- Studio
- Flutter

Core Tool Sets

- GMS
- App Store
- GOTA

Core service/apps

- FFMPEG
- OPENCV
- TFLITE
- Barcode scan
- …

3rd libs

- JetPack
- AliSDK
- Facebook SDK
- Face++ SDK
- Unity
- …

3rd SDKs

- Alipay
- Tiktok
- Facebook
- Snapchat

Popular applications

AOSP Android

SOC Android BSP

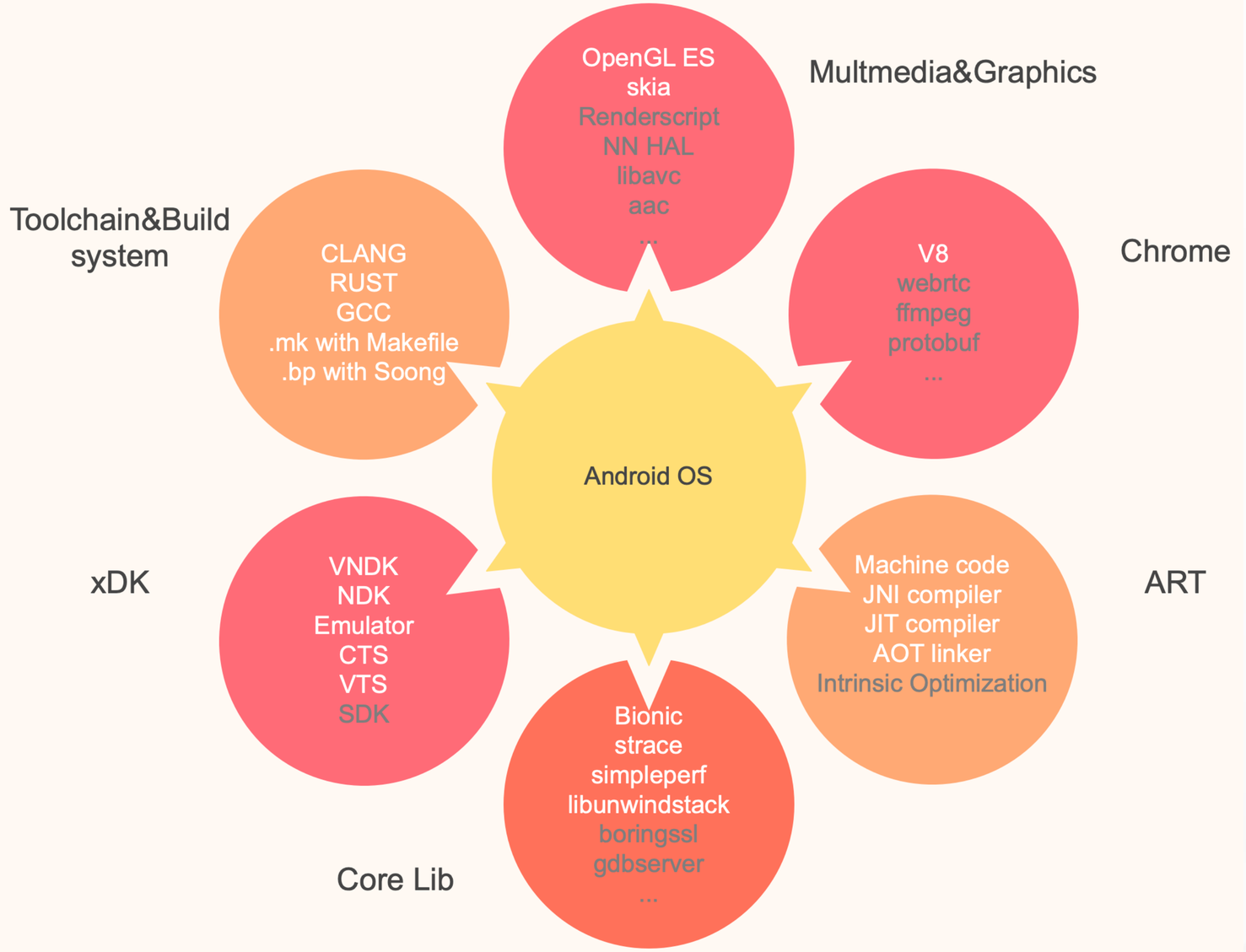
Device Android BSP

# Android Porting Work Break Down

100+
Gits changed

2K+
File changed or added

100K+
Code lines changed or added



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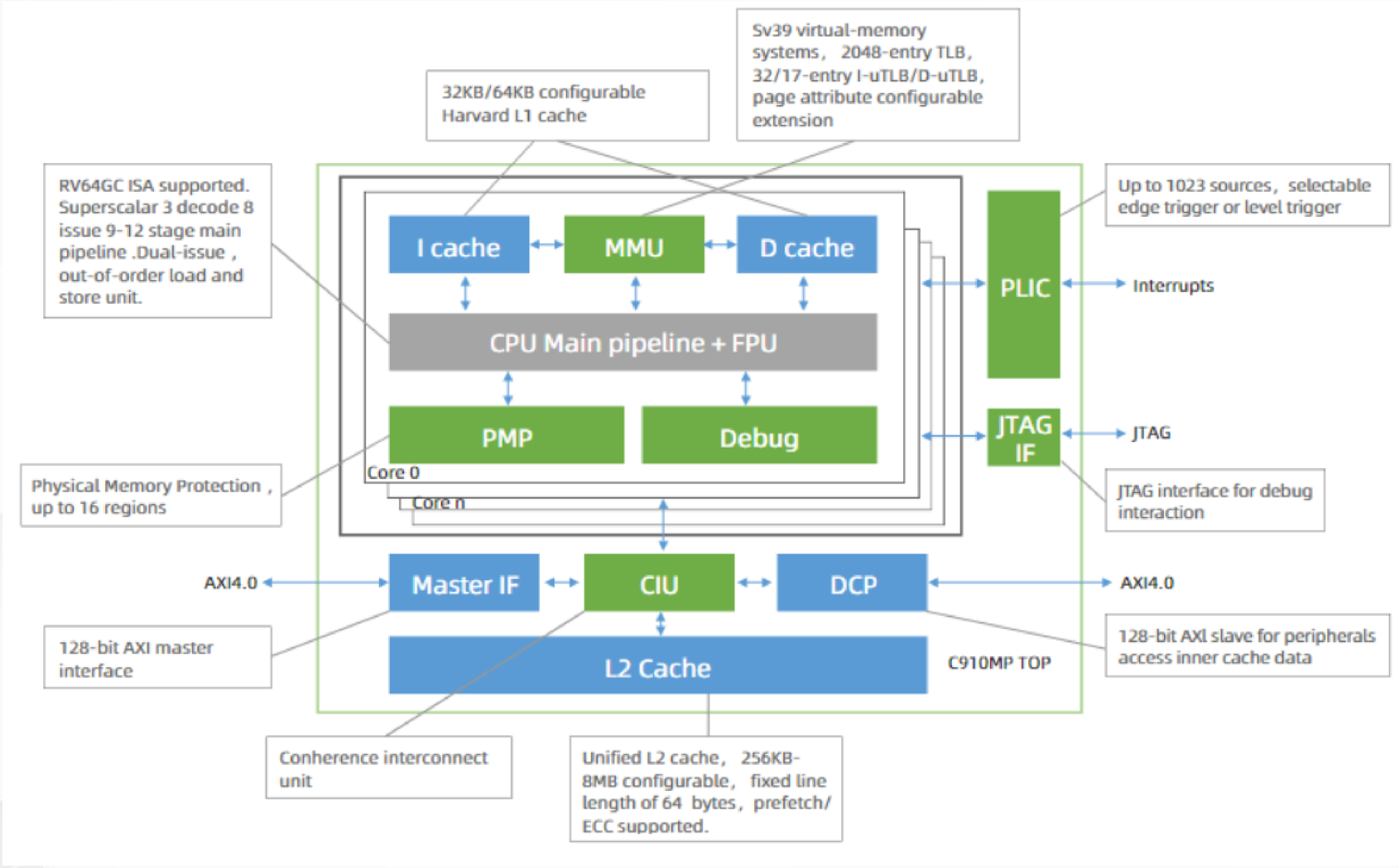
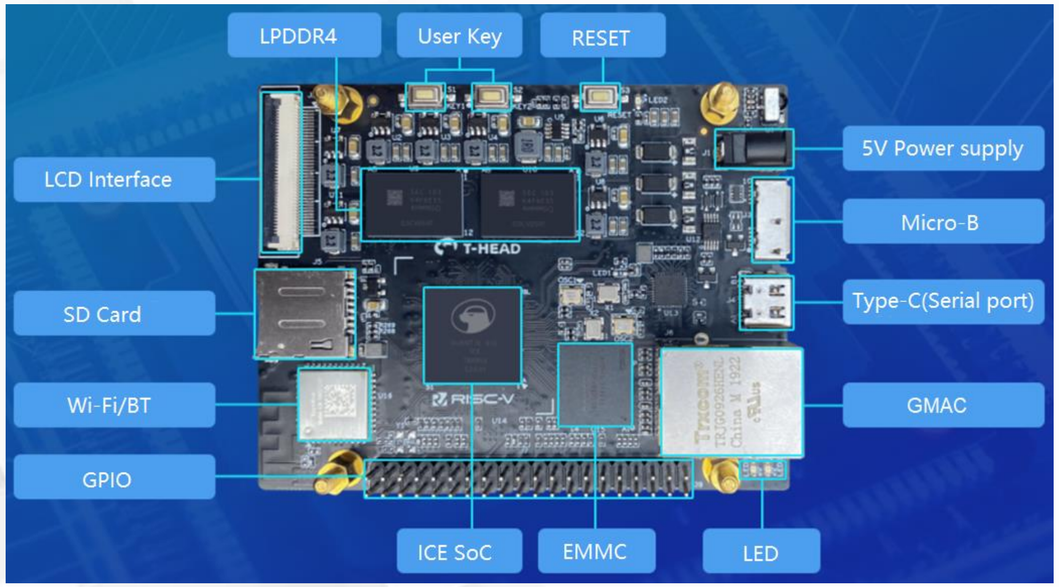
| Feature | Description |
|---|---|
| Architecture | RV64GC |
| SMP | Up to 4 cores in each cluster |
| Pipeline | 12 stages (Integer) |
| Floating-point Unit | Support RISC-V F, D instruction extension<br>Support IEEE 754-2008 standard |
| Bus interface | AXI4-128 master |
| Device coherence port | AXI4-128 slave (Optional) |
| Instruction Cache | Up to 64KB with optional parity |
| Data Cache | Up to 64KB with optional ECC |
| L2 Cache | Up to 8MB with optional ECC<br>Supporting parallel access with multi-bank |
| XuanTie extensions | XuanTie Instruction Extension（XIE）<br>XuanTie Memory Attributes Extension（XMAE） |
| Memory Management Unit (MMU) | Sv39 virtual memory translation<br>Up to 2048 entry TLB |
| PMP | Up to 16 regions |
| Interrupt Controller | Flexibly configurable Platform-Level Interrupt Controller (PLIC) for supporting wide range of system event scenarios |


Sv39 virtual-memory systems, 2048-entry TLB, 32/17-entry I-uTLB/D-uTLB, page attribute configurable extension
32KB/64KB configurable Harvard L1 cache
RV64GC ISA supported. Superscalar 3 decode 8 issue 9-12 stage main pipeline .Dual-issue , out-of-order load and store unit.
Up to 1023 sources, selectable edge trigger or level trigger
I cache
MMU
D cache
PLIC
Interrupts
CPU Main pipeline + FPU
PMP
Debug
JTAG IF
JTAG
Physical Memory Protection , up to 16 regions
Core 0
Core n
JTAG interface for debug interaction
AXI4.0
Master IF
CIU
DCP
AXI4.0
128-bit AXI master interface
L2 Cache
C910MP TOP
128-bit AXI slave for peripherals access inner cache data
Conherence interconnect unit
Unified L2 cache, 256KB-8MB configurable, fixed line length of 64 bytes, prefetch/ ECC supported.

# SoC Platform and Android Related Configuration


## Hardware: RVB-ICE

- Dual Core XuanTie C910(rv64imafdc)
- 4G DDR4
- GPU graphics rendering
- Available for online evaluation & Pre-order




## Software:

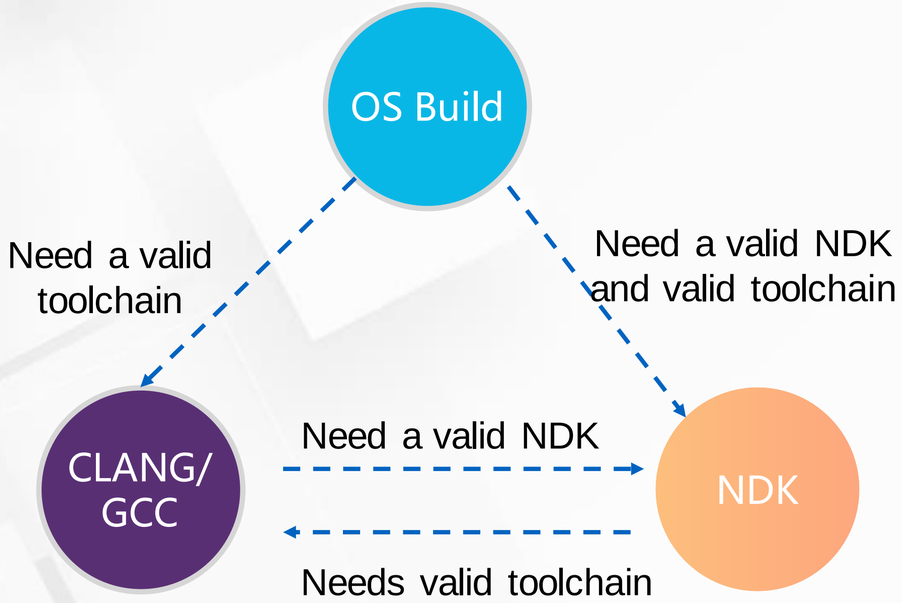
- Android 10
- Kernel 5.4.57

## Features

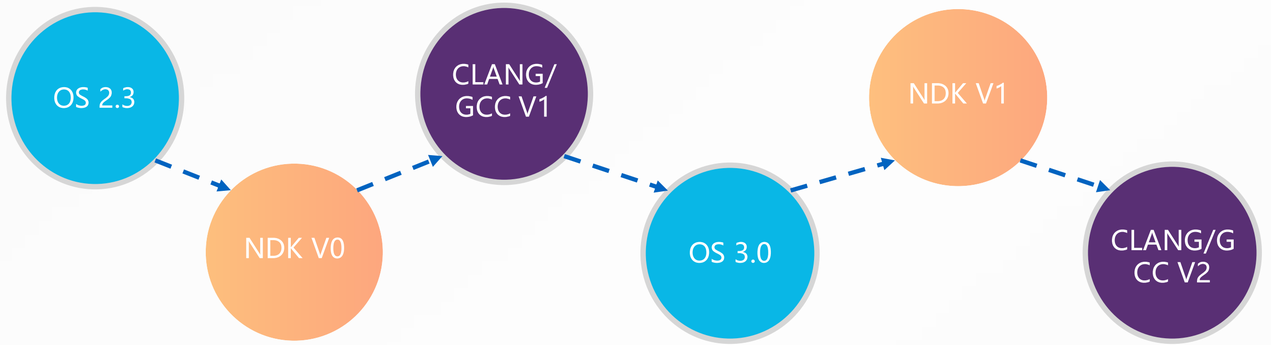
- ✓ Android Java runtime and most native service are enabled and running
- ✓ Basic boot to Android launcher with simple Applications
- ✓ Emulator and T-HEAD ICE SoC Boot
- × No 32bit support
- × “lto/thin/float16” clang features not be supported
- × Most of software a/v codecs disabled
- × RenderScript disabled
- × Neural Network feature disabled

# Toolchain First or NDK First?

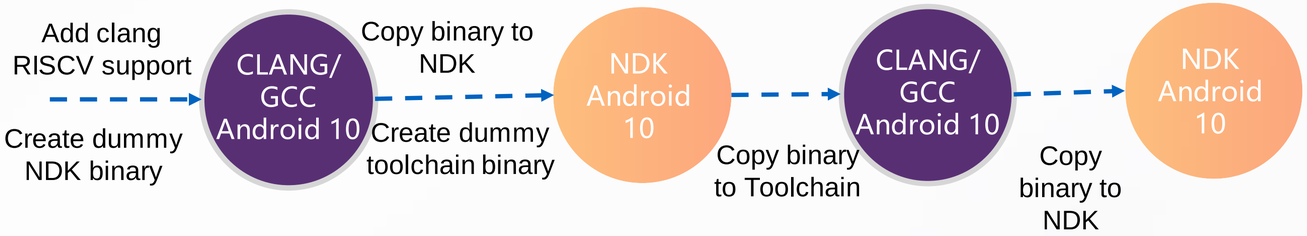
## Build Toolchain first or NDK first？




## How does ARM build work？




## How does RISC-V build work？



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# RISC-V Android OS Porting

| Assembler | Disassembler | Runtime | JNI | Jit compiler | AOT |
|---|---|---|---|---|---|
| • IR assembly<br>• Assembly micro | • Instruction Info array | • CXX_interp<br>  • Runtime mode switch<br>  • context saving<br>• Mterp<br>  • bytecode handler | • JNI Macro assembler<br>• JNI calling convention | • InstructionCode GeneratorRISC V64<br>• Intrinsic | • AOT compiler<br>• AOT linker |

ART: 50k+ code added

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# RISC-V Android OS Porting

| Base | 3rd party | V8 |
| --- | --- | --- |
| • APK<br>• LLVM<br>• build | • angle<br>• blink<br>• ffmpeg<br>• libjpeg_trubo<br>• libvpx<br>• protobuf | • Built in Optimization<br>• Optimization with RISC-V extension |

Chrome: 40k+ code added

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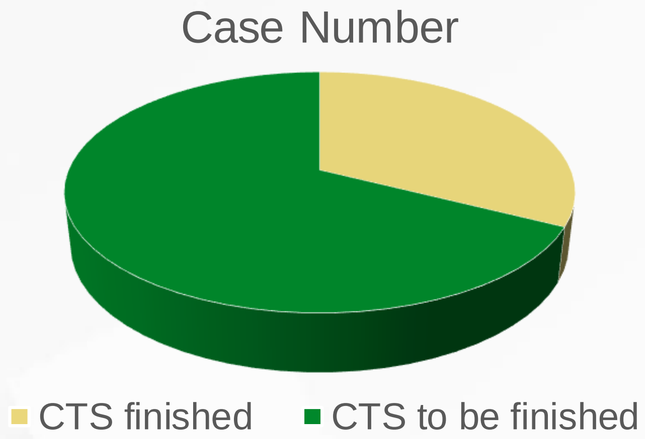
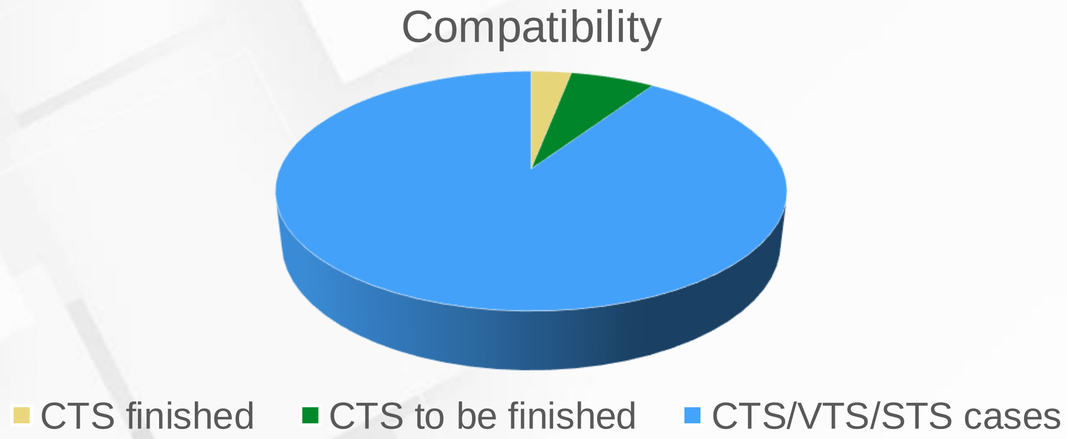
# RISC-V Android OS Porting

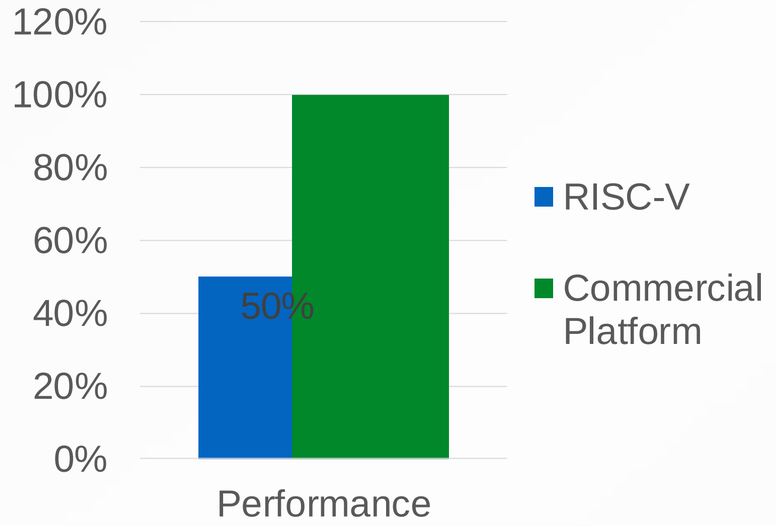
| Bionic | Support lib | Toolchain |
| --- | --- | --- |
| • Syscall generation<br>• linker<br>• RISC-V kernel header<br>• mem/str APIs optimization | • OpenGL ES<br>  • Assembly API call<br>• libbacktrace<br>• libunwindstack<br>• debuggerd<br>• libmemunreachable | • Clang 11<br>• GCC 8.1<br>• NDK r20 |

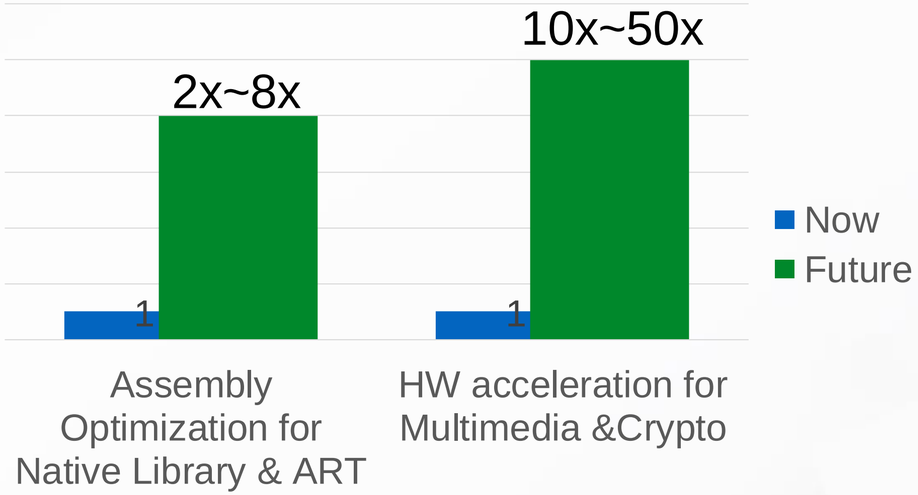
Miscellaneous: 10k+ code added

# Status


Case Number
CTS finished
CTS to be finished


Compatibility
CTS finished
CTS to be finished
CTS/VTS/STS cases


120%
100%
80%
60%
40%
20%
0%
50%
Performance
RISC-V
Commercial Platform


2x~8x
10x~50x
1
1
Assembly Optimization for Native Library & ART
HW acceleration for Multimedia &Crypto
Now
Future

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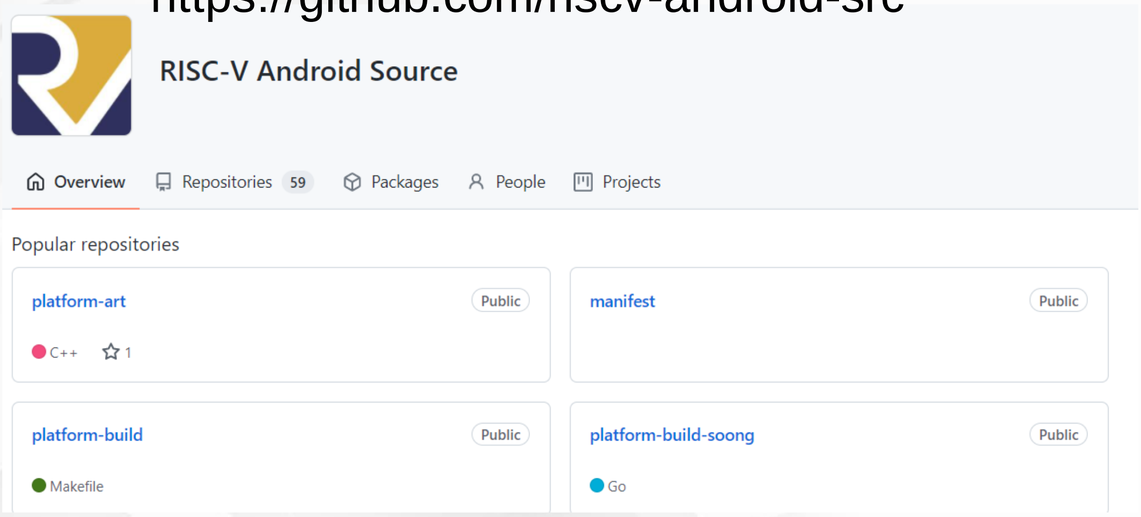
## Open chip community (English page):

occ.t-head.cn/community/risc_v_en

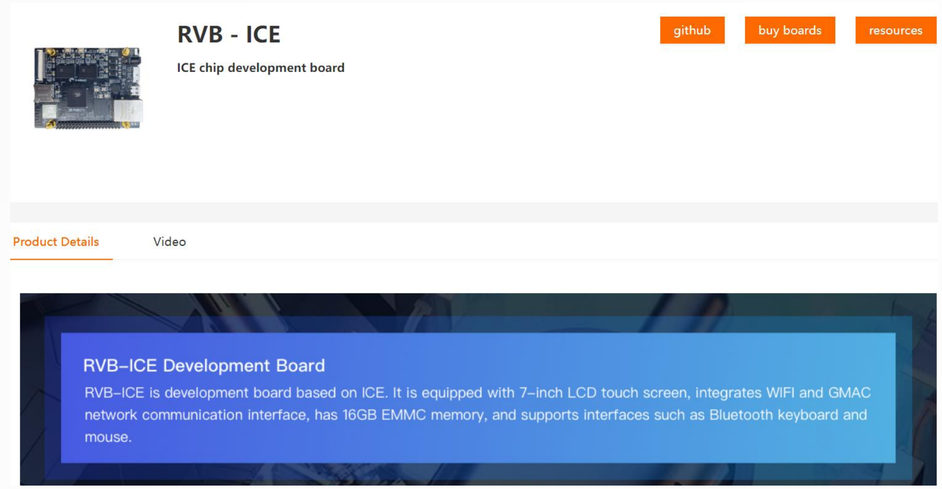

## Look for the codes/binaries :

https://github.com/riscv-android-src



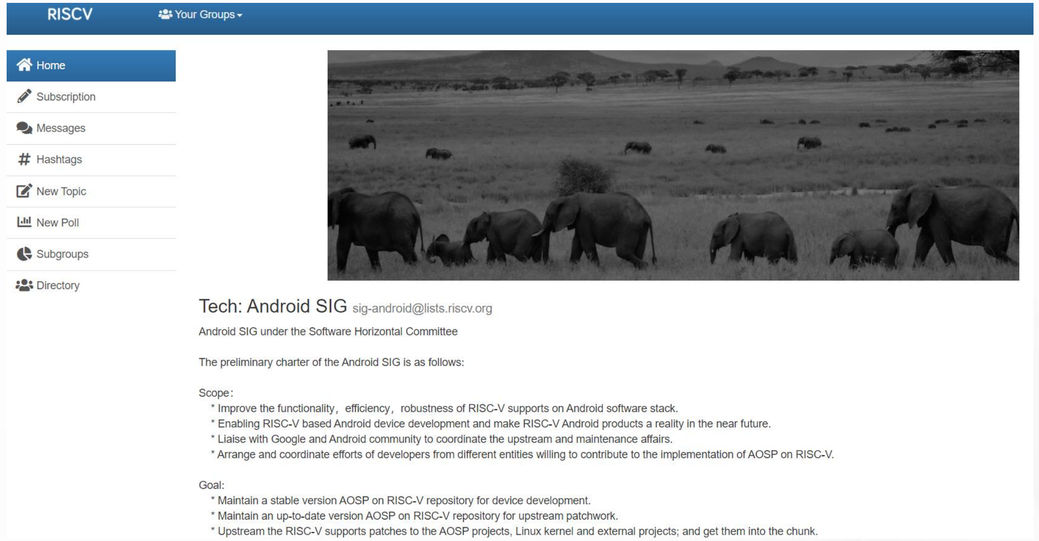

## Order the board:

occ.t-head.cn/community/risc_v_en/detail?id=RVB-ICE




## Join the discussion:

https://lists.riscv.org/g/sig-android



# RISC-V Android SIG


We need you!

Android SIG

Github

Developing Hardware

Group Forum

Regular Meeting

AOSP Android

# THANK YOU