CHIPS ALLIANCE AND THE OPEN HARDWARE LANDSCAPE

THE LINUX FOUNDATION

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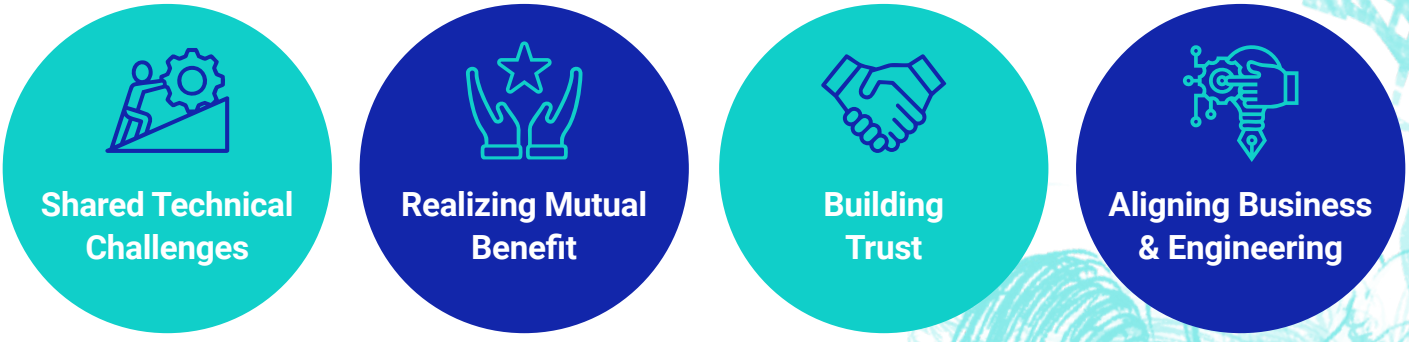
THE NEED FOR OPEN HARDWARE

Open-source software has shown impressive growth in the technology industry, academia, and for personal use over the past three decades. It has led to increased innovation, decreased cost for software, and the freedoms that are fundamental to the Open Source movement: to use, study, copy, modify, and redistribute code. Open-source software has seen a ubiquitous adoption because of these benefits and freedoms. While many open-hardware projects and organizations have also formed over the past few decades, the Open Hardware movement has not seen the same broad adoption. The goal of CHIPS Alliance is to accelerate the adoption of Open Hardware and to encourage innovation in hardware design.

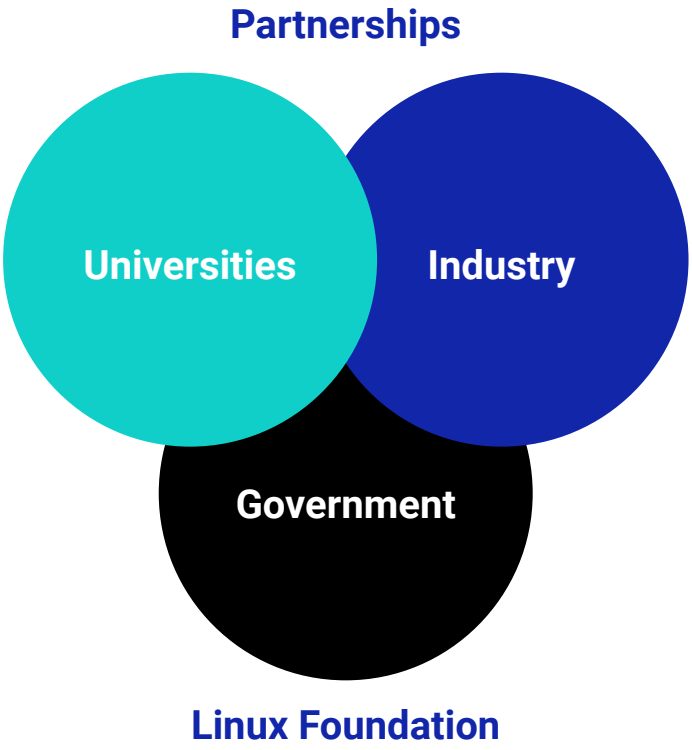
This requires a fundamental shift in how companies design their hardware, collaborate with their customers/competitors, and how they create supply chains. Open software development, component usage, and integration at higher levels of functionality has occurred over the past 30 years because of a similar business realization. At the heart of this though, is trust between collaborating organizations.

As the chart below shows, open hardware collaboration requires the alignment of business, technical, and legal objectives to enable cooperation between competing entities on areas of shared challenges. In some regards, this is the first step, beyond donation of building block IP, to enable the creation of higher level functionality.

Making Collaboration Work



CHIPS Alliance, as part of the Linux Foundation, offers a neutral territory for organizations to come together and collaborate on problems of mutual interest in the semiconductor, chip design, and EDA space together.



The Difficulty in Broad Hardware Definitions

The comparably weak adoption of open-hardware products is due in part to the difficulty in aligning the technology industry's efforts around broad definitions. Organizations often work best when basing their work on standards, dividing their efforts into verticals, and strictly defining the interactions between those verticals. Innovation often occurs when groups work outside this structure, explore new possibilities, and integrate the innovation back into the organization. The path to innovation with open-hardware projects may be quite clear, however with no strict definition of "open-hardware" projects, reintegration may prove impossible. Time will be lost in defining which parts of the hardware project are "open", what licenses can be used, having trust in open-source hardware IP, and finally understanding / managing risk. If these barriers to adoption cannot be overcome expediently, any benefit to adoption of innovation may be lost to a constantly changing and evolving market.

THE CHIPS ALLIANCE MISSION

The mission of CHIPS Alliance is to restrict ourselves to a narrow definition of Open Hardware, to create best practices for adoption of these technologies, and to foster communities around the projects within the scope of our definition. As such, CHIPS Alliance will focus our efforts on the following types of Open Hardware:

- Hardware Implementations: SoCs, Buses, Accelerators, and I/O blocks
- FPGA & ASIC Tooling
- HDLs and Verilog Generators
- Open Source PDKs

By restricting ourselves to these types of hardware, we hope to foster collaboration, share the cost of development, reduce licensing fees, and accelerate innovation in hardware design.

Benefits to Industry

The benefits we hope to achieve mirror that of the Open Source movement in general and open-source software in particular. However, it is worth calling out how these concepts can benefit the industry when applied to our restricted definition of Open Hardware.

The core benefits to larger organizations include cost efficiency, quality of innovation, strategic flexibility, and market positioning. Organizations can share the R&D costs of developing RTL designs with the community, reducing overall expenditure. Likewise, organizations will see reduced reliance on single vendors and the ability to switch suppliers or integrate diverse technologies more easily. We hope to position projects such that the open-source designs are flexible and can be used as a foundation for products. Collaborative development leads to extensive peer review and testing, often improving the quality and reliability of designs. Open-source projects benefit from a global pool of contributors, leading to faster innovation cycles. These benefits all come with a required commitment to transparency and collaboration that can drive industry-wide adoption and interoperability of designs.

Benefits to Startups

CHIPS Alliance endeavors to benefit organizations of all sizes. Smaller organizations can benefit from lowered barriers to entry, access to niche expertise in design, and the flexibility/scalability that comes with open-source projects. Access to high-quality RTL designs without the need for expensive licenses significantly reduces costs, while speeding up development and allowing companies to bring products to market more quickly. Expertise in complex hardware design is generally relegated to the organizations that can afford the cost of bringing those designs to market. We hope to encourage access to experienced developers by building strong communities around CHIPS Alliance projects.

Benefits to Hardware Freedom

The Open Hardware movement promotes the freedom to modify and adapt RTL designs to better suit the specific needs and preferences of the individual. This can be a valuable learning resource for hobbyists and individuals interested in electronics and design. This is one of the core tenants of an Open Source methodology, and extends from academic to personal use.

CHALLENGES FACING OPEN HARDWARE

The barriers to large-scale adoption of open hardware are significant, involving technical, economic, legal, and cultural challenges. Specifically for RTL designs, overcoming these barriers will require advancements in verification and validation tools, clearer licensing frameworks, and cultural shifts within the industry towards open collaboration.

Overcoming Barriers to Entry

It is our hope that the projects we foster will show value in areas which lead organizations and communities alike to embrace Open Hardware. These barriers include verification/validation cost and complexity, integrating open-source RTL with existing designs, and creating an ecosystem of interoperable designs. The key to overcoming these and other barriers will be the strength of the communities that develop around projects.

Fostering a Community First Model

Open-source code without a community to support it rots in much the same way any physical structure will, starting with the exterior, or public interface. CHIPS Alliance engages with projects to enable their participation in conferences, hackathons, and meetups in order to help foster a sense of community and shared purpose among developers. CHIPS is also engaged in tooling for the benefit of the communities. GitHub is perhaps the most obvious example of a platform based on a software tool which has allowed millions of developers to work together on projects, fix bugs, and generally improve software collectively. CHIPS focus on FPGA & ASIC tooling hopes to enable similar workflows to become standardized across the industry.

Encouraging Hardware-Software Co-Design

In a digital systems design software executes on the hardware components. Hardware and software co-design can be defined as meeting system level objectives by exploiting the cooperation between hardware and software as concurrent design components. Most silicon implementations today also require software support, typically a Board Support Package (BSP) which provides essential support for silicon features implemented by chips used in hardware platforms. This provides a level of hardware abstraction that allows software to run on different architectures. This approach is followed by several open-source software projects like Linux, Yocto, Zephyr, FreeRTOS just to name a few.

Hardware-software co-design allows hardware and software components to be developed simultaneously instead of sequentially and has several benefits:

- **Optimized performance, power consumption and cost**
- **Faster prototyping using both FPGA emulation and software simulation**
- **Design abstraction providing better integration of hardware and software**
- **More efficient communication protocols between hardware & software with well-defined APIs**
- **Integrated tooling support for development, simulation, synthesis, and debugging**

Several projects require analysis at design time in order to create an architecture where implementation of critical algorithms is divided between silicon and software to achieve optimal performance.

This approach has already been proved successful by the SONiC project. This hardware-software co-design initiative focused on networking software for switches has allowed a faster time-to-market for new hardware designs where performance and ecological footprint is highly dependent on software and hardware interaction.

THE OPEN HARDWARE COMMUNITY

Open Hardware Standards

There are numerous organizations involved in various aspects of open-hardware specifications and standards. These organizations focus on details ranging from the instruction set architecture to interface signals between small chips (chipsets) packaged together.

Open hardware standards provide a way for communities aligned in a common interest area to collaborate on the design and development of a specification that can be standardized in industry. Different organizations foster and host the development of such specifications and standards in different ways.

Example Open Standards Groups

Accellera develops and promotes standards for chip design verification including functional power, test, clock domain crossings, as well as standards related to design implementation languages, such as SystemC and SystemVerilog. Accellera works closely with IEEE for standards development.

IEEE fosters and hosts the development of a number of specifications in the hardware design space, chip design description languages, and cell library models to name only a few.

OpenPOWER focuses on the development and adaptation of the POWER ISA primarily for datacenter type workloads.

RISC-V focuses on the development and adoption of the RISC-V ISA from IoT, to mobile, to data center type workloads. RISC-V does not provide any reference implementations, but rather relies upon the community to implement its specified design.

Open Compute Project (OCP) focuses on a broad spectrum of technical compute challenges, primarily relating to all aspects of the data center. OCP provides a platform for collaborative specification development and hosting.

SI2 provides collaborative technology and services which enable higher levels of semiconductor design integration leading to industry-accepted standards. It is the intent of this initiative to make any such standards, technology, and services available to all who are interested at a fair and reasonable cost.

UCIE focuses on the electrical and logical specification for inter-die chiplet communication. An earlier version of this specification known as AIB was originally donated by Intel to CHIPS Alliance, where it is still hosted.

Open Hardware Organizations

The Open Hardware ecosystem is quite diverse, and this is evident from the wide variety of organizations that have grown to support the effort. Below is a non-exhaustive list of representative organizations that are provided as examples: these range from non-profit to for-profit companies, and include interests ranging from embedded hardware/software, EDA tools, open-source hardware implementations, to selling hardware based on open-source designs. CHIPS Alliance gives these organizations a place to align their efforts, while providing a flexible charter for collaborating on projects. It is through this flexibly that we see our differentiation: providing a home for projects that might not fit in other communities.

Example Open Hardware Organizations

The OpenHW Group, part of the Eclipse foundation, focuses primarily on the design and development of RISC-V cores using proprietary EDA tools for their construction and verification. These cores are then used by industries who already rely on these tools.

OSHWA's goal is to foster technical knowledge and encourage research that is accessible, collaborative, and respects a user's freedom. The main activity is the hosting of the annual Open Hardware Summit, and maintaining the Open Source Hardware certification.

KiCad is a hierarchical schematic editor from schematics to PCB's.

Arduino is an open-source electronics platform that is based upon easy to use hardware and software. The goal is to make its hardware and software readily approachable, hence an excellent vehicle for both students and professionals alike.

Sparkfun is a reseller aimed at hobbyists and educators for electronic parts for constructing electronics. All products designed and produced by SparkFun are released as open-source hardware including schematics, EAGLE files, and datasheets posted on each product page.

Antmicro is a software-driven tech company developing edge computing systems for various branches of industry. As a company, as well as individually, they are active in open software and open hardware, which they consider a strong foundation for transparent, shared development processes based on good practices.

How CHIPS Alliance is Different

CHIPS Alliance collaborates with many of these organizations, however we see ourselves as different by focusing on four distinct traits of Open Hardware:

CHIPS is Free as in Freedom

CHIPS Alliance welcomes participation and collaboration amongst companies, universities, and individuals. It does not require membership in the Linux Foundation or CHIPS Alliance, contribution of IP, or assignment of quantified resources for participation. Participation in some aspects of CHIPS may require signing a Contribution Level Agreement as described here.

End-to-End Open: From Hardware to Firmware

CHIPS Alliance promotes and supports collaborative development spanning the architecture, the process design kits (PDKs), and the EDA software applications that enable chip design. CHIPS Github repositories include numerous examples of IP that is under Apache 2.0 license and can be used for building larger SoC designs.

Standards and Implementations

While CHIPS has been host to standards creation and promotion, such as the AIB chiplet protocol initially provided by Intel, we promote an overall open-source chip ecosystem to enable the collaborative creation and development of semiconductor IP.

All Cores Welcome: Large or Small

CHIPS hosts and works on a number of different SoC blocks. These include larger RTL designs of full RISC-V cores as well as smaller in-silicon designs deployed in cloud data centers.

All Are Welcome: Hobbyist, Tinkerers, and Companies of All Sizes

CHIPS is seeking to build a professional environment for both research as well as commercial product development. As such, the objective is to build high quality IP that can be used and trusted from a business, technical, and legal perspective. However, most importantly, CHIPS encourages the collaboration of hobbyists or folks new to hardware design. Much like the Linux kernel, we realize that it takes a village to support an open-source project.

DEFINITIONS

AIB (Advanced Interface Bus): A chiplet communication protocol initially developed by Intel and later donated to CHIPS Alliance.

ASIC (Application-Specific Integrated Circuit): A chip designed for a specific application rather than general-purpose use.

BSP (Board Support Package): Software that provides low-level support for a specific hardware platform, facilitating system abstraction for software developers.

FPGA (Field-Programmable Gate Array): A reconfigurable hardware device used for prototyping or specialized computing tasks.

HDL (Hardware Description Language): Programming languages, such as Verilog, used to model hardware components and systems.

Hardware-Software Co-Design: A concurrent development approach for hardware and software to optimize system-level performance.

Open Source PDK (Process Design Kit): Collections of files and guidelines used for semiconductor manufacturing, openly available to support hardware design without proprietary restrictions.

RTL (Register Transfer Level): A design abstraction in digital circuit design focusing on data flow between registers.

SoC (System-on-Chip): Integrated circuits that incorporate multiple components like CPUs, memory, and input/output interfaces on a single chip.